Strong Fermi-level Pinning Driven by Epitaxial Graphene Interlayer in Metal/4H-SiC Junction

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Fermi-level pinning is a phenomenon that the Schottky barrier of metal/semiconductor junction exhibits weak dependence on the metal work-function. According to the previous study [1], the metal/graphene/Si junction exhibits strong Fermi-level pinning which is expected on an ideal metal/Si junction. It has been reported that the Fermi-level pinning of metal/SiC junction is relatively weak compared with the metal/Si junction due to the ionicity between atomic elements of crystalline structure [2]. With this background, we investigated the Fermi-level pinning in metal/graphene/4H-SiC junctions. The junction was fabricated by first epitaxially growing graphene on a 4H-SiC substrate with the metal-capping method under UHV environment [3] and then depositing circular metal (Al, Ni, Pt) electrodes onto the grown graphene layer. The Fermi-level pinning factor S was extracted from current-voltage (I-V) and capacitance-voltage (C-V) curves, signifying strong Fermi-level pinning. A theoretical model proposed by Kopylov *et al*. describing the charge transfer at the graphene/SiC interface provides a plausible explanation for the observed strong Fermi-level pinning [4].

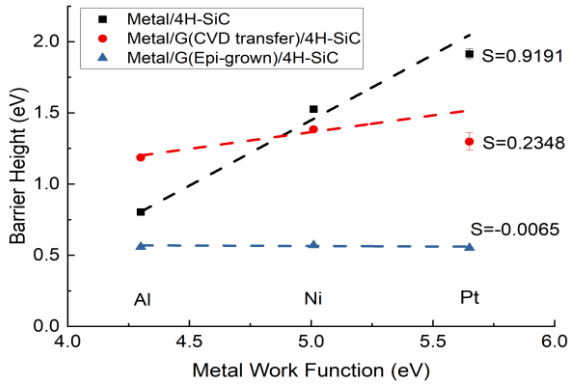

Figure 1 Schottky barriers of fabricated devices obtained from I-V measurements vs. metal work-function

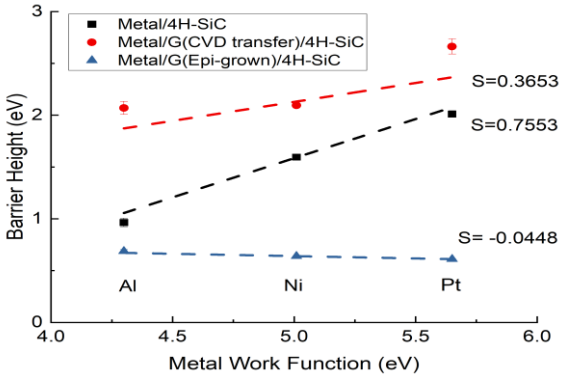

Figure 2 Schottky barriers of fabricated devices obtained from C-V measurements *vs*. metal work-function

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NRF-2023R1A2C1006519, NRF-2022M3K2A1083924