Improving Hot Electron-Induced Punchthrough (HEIP) via Dual STI Sidewall Process in DRAM

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As device scaling continues, higher electric fields develop in MOSFETs, leading to the generation of hot carriers in the channel and increased off-current due to hot-electron-induced punchthrough (HEIP) in pMOSFETs [1]. In low-power DRAM, minimizing pMOSFET off-current is crucial to reducing standby power consumption, making HEIP immunity improvement essential for meeting standby current requirements. The primary factor behind HEIP degradation is electron trapping in the top region of the STI liner nitride. To enhance HEIP immunity, solutions such as increasing the gate length using a large tabbed-gate design or thickening the STI sidewall oxide to reduce electron trapping in the STI liner nitride have been proposed. However, while a large tabbed-gate design can improve HEIP immunity, it also increases chip size, making it impractical for low-power applications. A thicker STI sidewall oxide is a more viable solution, offering improved HEIP immunity without degrading DRAM performance. Nonetheless, in 10nm-scale DRAM products, increasing the core STI sidewall oxide thickness transforms the long-axis cell STI structure from an oxide-nitride configuration to a fully oxide-filled structure. This shift causes abnormal recess formation during cell gate fin patterning, resulting in VTS variability degradation. This paper presents and validates a process method that increases the core sidewall oxide thickness to improve HEIP immunity while maintaining the oxide-nitride structure in the cell STI region, which is critical for optimizing fin pattern formation.

[1] K. Kim *et al.* Microelectron. Reliab. (2002)