Studying the nucleation of GaP on v-grooved Si for III-V/Si device integration

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The direct heteroepitaxy of III-V materials on Si for high efficiency optoelectronic and photovoltaic applications has progressed greatly in recent years, but most studies have focused on polished wafers, that are compatible with microelectronics (e.g. CMOS) fabrication, but not photovoltaic technologies. There has been recent interest in growing III-Vs on "v-grooved" surfaces, where nanoscale patterning and facet selective etching is used to pattern nominally (001) Si surfaces with linear (111)-facetted v-groove structures. This v-grooved geometry suppresses antiphase boundaries (APBs), thereby enabling defect-free nucleation of polar III-V materials on nonpolar Si. However, for applications where cost is important, it also brings with it the challenge of creating the v-grooved pattern in a cost-effective way, without an expensive wafer-polishing step.

In this work, we show how v-groove structures can be prepared with cost-effective patterning approaches (nanoimprint lithography and interference lithography) on unpolished Si surfaces.[1] Unlike prior studies of growth of III-Vs on v-groove structures, which have focused on lattice mismatched heteroepitaxy of III-Vs (GaAs, InP, etc.), we have focused on GaP, which has a very small lattice mismatch with Si and enables us to understand the fundamentals of III-V nucleation on partially v-grooved surfaces, where multiple facets are exposed during growth. This is also an excellent platform to investigate the coalescence of selective area growth, a topic that is important for large-area applications such as photovoltaics.[2] We have systematically studied the nucleation conditions for GaP on v-groove Si and identified conditions that enable facet-selective nucleation without the formation of APBs, and lead to smooth, planar coalesced films.

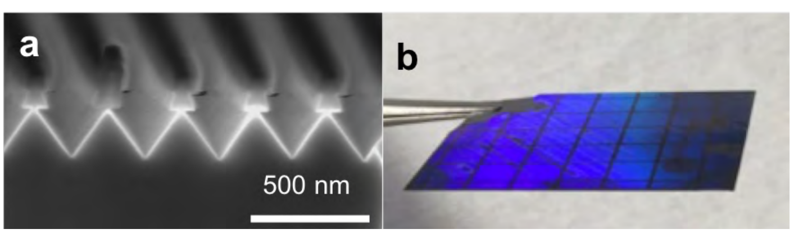

Figure 1 a) SEM of v-grooved Si with NIL resist still present; b) optical image of NIL-patterned unpolished Si

[1] E.L. Warren et al, Proc. IEEE PVSC, (2018).
[2] W.E. McMahon et al, APL Materials, (2018).

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