Nitrogen Doping of Gallium Oxide by Ion Implantation and Its Application to Vertical Transistors

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β-gallium oxide (β-Ga_2O_3) has a very large bandgap (~4.5 eV) and a breakdown electric field exceeding 6 MV/cm, making it an attractive candidate for next-generation power electronics. However, Ga_2O_3 has a fundamental physical drawback, namely a lack of hole-conductive *p*-type material, because of unavailability of shallow acceptors, a valence band structure mostly formed by O 2*p* orbitals, and a self-trapping effect of free holes. Recently, we succeeded in developing a nitrogen (N)-ion-implantation doping process for Ga_2O_3 to form an energy barrier in a device structure [1] and then fabricating vertical Ga_2O_3 transistors by using a device process based on the N-ion implantation doping [2, 3].

N atoms are theoretically expected to be a deep acceptor in Ga_2O_3. We performed N-ion implantation doping into an *n*-Ga_2O_3 layer to fabricate a current blocking layer by forming a Si-doped–N-doped–Si-doped Ga_2O_3 *n*-*p*-*n* junction. Note that Si is a shallow donor with an activation energy of about 50 meV in Ga_2O_3. Then, depletion-mode (D-mode) and enhancement-mode (E-mode) vertical Ga_2O_3 transistors with a current aperture were fabricated by using a manufacturable all-ion-implanted process, which is similar to commercial Si and SiC power device technologies, with Si and N doping. Both the D-mode and E-mode devices demonstrated successful transistor action and decent device characteristics. A schematic cross section and DC current–voltage (*I*–*V*) output characteristics of a typical D-mode transistor are shown in Figs. 1 and 2, respectively.

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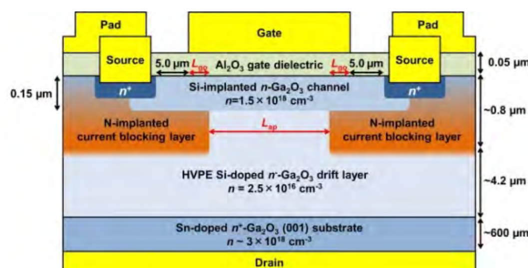

Figure 1. Cross-sectional schematic of D-mode vertical Ga_2O_3 transistor structure: L_{ap}=20 µm and L_{go}=2.5 µm.

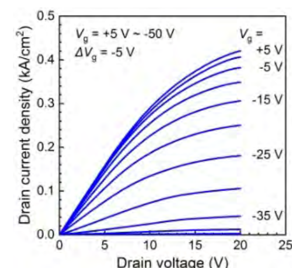

Figure 2. DC *I*–*V* characteristics of D-mode vertical Ga_2O_3 transistor.

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