Emerging Memory Technologies and the Future of Computing

M.J. Marinella+

Sandia National Laboratories, Albuquerque, NM 87185

The most significant bottleneck in modern computing is that between the processing and storage of information. Decades of improvement in microprocessor technology have rendered the energy and time requirements for computation insignificant compared to those for reading and writing to off-chip main memory and storage. Improvements in computational efficiency are now swamped at the system level by memory access – and solving this von-Neumann bottleneck is one of the key challenges to enable the next generation of computing. Fortunately, several compelling memory technologies are emerging which may solve this challenge. Chief among these are a class of devices in which the state of the memory is stored as the resistance across its terminals. These technologies include redox resistive memory (ReRAM), conducting bridge memory (CBRAM), phase change memory (PCRAM), ferroelectric tunnel junctions (FTJ), and spin transfer torque (STT-RAM). All of these technologies can be integrated into the back end of line with a standard CMOS logic process. Monolithic integration of memory with logic drastically reduces the latency and energy of memory access. Voltage controlled technologies like ReRAM, CBRAM, and PCRAM can be configured in a dense crossbar with an area as small as $4F^2$ when using an inline select device (where F is the minimum lithographic feature size). When layered, these devices can reach densities of 100 terabits per cm^2, which can enable extraordinarily dense information storage integrated close to the computation. Magnetic and ferroelectric memories are capable of nearly infinite endurance with a very low switching energy, and hence may offer a replacement for the large SRAM cell for caches. It is also possible to use emerging memories to perform logic operations, further increasing the efficiency and performance of a computing system. However, several challenges remain before the full potential of emerging memory technologies will be realized. Chief among these are improving retention, endurance, and bit error rates through better understanding of the basic physics of switching. In addition, the development of suitable in-line select devices will be required to enable maximum density. This presentation will discuss the basic physical mechanisms, state of the art, and future prospects for these key emerging memory technologies and their role in the Beyond Moore era of computing.

+ Author for correspondence: mmarine@sandia.gov

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