

Fig. 1. (a)-(c) Cross-sectional schematics after 20, 350, and 1300 nm of p-InP (p=10<sup>18</sup>cm<sup>-3</sup>) growth on patterned n-InP substrate. Pattern consists of isosceles-right-triangles (side length = 965 nm) of SiN (40 nm thick); (d) plan-view SEM after 20 nm growth showing selectivity; (e) and (f) XSEM after 350 and 1300 nm of p-InP growth.

## 20 nm InP growth

## 350 nm InP growth 1300 nm InP growth (a) 1110 nm triangle 110 nm triangle 1110 nm triangle No TD, SF ghest SFD No III-V on dielectric TDD = 4.2×10<sup>7</sup> cm<sup>-2</sup> p-InP pits SiN TDs h) 465 nm triangle (b) 465 nm triang $TDD = 9.7 \times 10^7 \text{ cm}^{-2}$ TD on dielect V-III O TDs pit (i) 266 nm polygon 66 nm polygon (f) 266 nm polygo 1 µm owest SFD, TD **III-V on dielec** $TDD = 5.0 \times 10^6 \text{ cm}^{-2}$ TDs ECCI ECCI SEI ECC SE

Fig. 2. (a) - (c) ECCI/SEI of 20 nm p-InP grown on patterned SiN/n-InP substrate with feature size of (a) 1110 nm, (b) 465 nm, and (c) 266 nm; (d) - (f) ECCI/SEI of 350 nm p-InP grown on similar patterns; (g) - (i) ECCI/SEI of 1300 nm p-InP grown on similar patterns. SF = Stacking fault, TD = threading dislocation, SFD/TDD refers to density. Scalebar = 1µm.



Fig. 3. (a) Plan-view schematics of patterned  $SiO_2/n-InP$  substrate (line pattern); (b) - (d) ECCI of 580 nm p-InP grown on the same substrate with  $SiO_2$  line oriented along (b) [0 -1 1], (c) [0 1 1], and (d) [0 1 0] crystallographic directions. Dashed line represent the two sides of buried  $SiO_2$  lines. The [0 1 0] stripes show the lowest defect density.

## References

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