International Workshop on Gallium Oxide and Related Materials (IWGO-6)
Room ESJ 0202 - Session IWGO-FrM2
Advanced Device Scaling and Fabrication Techniques II

Moderators: Samuel Graham, University of Maryland College Park, **Uttam Singisetti**, University of Buffalo

11:10am **IWGO-FrM2-39 High-Performance β-Ga_2O_3 Vertical Diodes and FinFETs with High Electric Field Strength***, **Sriram Krishnamoorthy**,* University of California at Santa Barbara **INVITED**

β-Ga_2O_3 holds immense potential for power device applications in the medium to high voltage regime, for power conversion using solid state transformers in AI data centers. **Trench Diodes:** We report on vertical Schottky barrier diodes (SBDs) based on *β*-Ga2O3 with trench architecture, featuring a high-permittivity dielectric RESURF structure. The incorporation of a trench geometry, coupled with the high-permittivity dielectric RESURF, effectively reduces the surface electric field at the metal-semiconductor junction. This reduction facilitates the use of a lower work-function anode contact, further diminishing the turn-on voltage. The combination of lower stored charge and a low forward voltage drop results in an excellent trade-off between conduction and switching power loss, yielding a QCVF figure of merit comparable to commercial bare die SiC SBDs. **Heterojunction Diodes:** Integration of p-type oxides with Gallium Oxide offer a way to circumvent the lack of p-type Gallium Oxide to increase built-in potential of junctions with lightly doped Gallium Oxide drift layers. We report on > 3 kV NiO and Cr_2O_3 heterojunction diodes with promising performance. > 1 A devices can be realized and double pulse testing of high current diodes with record low reverse recovery charge and time indicate the promise of topology. **Vertical Transistors:** A β-Ga_2O_3-based multi-fin vertical FinFET featuring a thick field oxide layer at the trench bottom to enhance the breakdown voltage will be discussed. With novel edge termination, we report a vertical FinFET with strategies to reduce electric field crowding around device edges, leading to enhanced breakdown voltages. To reduce the gate capacitance for superior switching performance, vertical FinFETs with split gate design are also fabricated. The devices are fabricated on (001) β-Ga_2O_3 HVPE epilayers grown on Sn-doped substrates. This approach of utilizing a vertical FinFET with split gate presents a promising solution for vertical power switches with enhanced breakdown capabilities and better switching performance. Using high voltage C-V measurements the drift layer thickness was extracted to be 11 µm, resulting in a record high average electric field of 3.1 MV/cm for the 3.4 kV FET, which is the *highest reported average electric field (V_{BR}/t_{drift}) in any vertical power transistor*, 3X the average fields in GaN and SiC vertical power transistors. Further improvements in β-Ga_2O_3 material and oxide quality will significantly enhance the performance of such devices with effective electric field management and edge termination.

11:35am **IWGO-FrM2-44 Diffusion Suppression of Mg and High Performance β-Ga_2O_3 Current Blocking Layers by N+Mg Co-Doping Approach***, **Fenfen Fenda Florena**, Hironobu Miyamoto, Yuki Koishikawa, Hirofumi Shinohara, Kohei Sasaki, Akito Kuramata,* NCT, Japan

Deep acceptor doping is a promising strategy for forming current-blocking layers (CBLs) in β-Ga_2O_3 vertical power devices, where p-type doping is not feasible. By compensating donor concentrations, deep acceptors create high-resistivity regions that mimic p-type body layers. While single Mg or N implantation has been demonstrated for CBL formation, these approaches suffer from high leakage current and premature breakdown. In Mg-implanted CBLs, profile distortion due to Mg diffusion during high-temperature post-implantation annealing (PIA) limits performance. To overcome these limitations, a co-doping approach have been explored theoretically to induce shallow acceptor levels via donor-acceptor level repulsion effect. This work presents the first experimental demonstration of N+Mg co-doping in β-Ga_2O_3 achieving improved CBL performance.

Multi-energy N and Mg implantations were introduced into β-Ga_2O_3 to form CBL, followed by PIA. Figure 1 shows the depth profile of N and Mg as revealed by secondary ion mass spectrometry (SIMS) measurement. At 1/1 depth ratio of N/Mg, alteration of Mg profile was detected due to massive Mg diffusion toward epilayer/substrate interface. Impressively, a remarkable Mg profile stability was achieved by implanting N much deeper into region (N/Mg = 2/1). Suppression of leakage current was more prominent in N+Mg co-implanted CBL compared to its single counterpart (more than two orders of magnitude) as shown in Fig. 2. Moreover, higher N/Mg depth ratio led to increase in breakdown voltage from 2.0 kV to 2.5 kV. This paper is based on results obtained from a project, JPNP22007, commissioned by the New Energy and Industrial Technology Development Organization (NEDO).

11:50am **IWGO-FrM2-47 >3.3 kV Ga_2O_3 Monolithic Bidirectional Switch: Impact of NiO/Ga2O3 Interface Charges***, **Yuan Qin**,* Virginia Tech*; Yuhao Zhang,* The University of Hong Kong, China

Bidirectional switches (BDSs), which block bipolar voltages in the off-state and conduct current in both directions in the on-state, are essential for AC power electronics [1]. Monolithic BDSs (MBDSs) with a shared drift region can reduce device area by about four times compared with solutions based on two discrete devices [2]. With its high critical electric field and superior thermal stability, ultra-wide-bandgap Ga_2O_3 is promising for high-voltage power devices, making it attractive for high-voltage power device applications. After earlier demonstrations of low-voltage Ga_2O_3 MBDSs [3], [4], we recently reported a JFET-based Ga_2O_3 MBDS with BV over 6.5 kV in both polarities [5]. However, its on-resistance (R_{on}) is still much higher than the ideal value predicted from channel resistivity analysis, and its reliability remains unclear.

This work investigates the R_{on} and reliability of a Ga_2O_3 MBDS, with a particular focus on the influence of NiO/Ga_2O_3 interface charges. The elevated R_{on} originates from the non-uniform current distribution caused by the NiO junction termination extension (JTE) and interfacial charges. Negative charges at the NiO/Ga_2O_3 interface are identified as the main factor responsible for the increased R_{on}. To assess the impact of these interface charges on long-term device reliability, reverse-bias stress tests at 3.3 kV were conducted. The minimal parametric drifts observed suggest that these interface charges correspond to deep-level traps and do not substantially affect the device's long-term performance. These findings offer valuable insights and guidelines for further optimizing the figure of merit of high-voltage lateral Ga_2O_3 devices.

[1] B. J. Baliga,IEEE Power Electron. Mag. **10**, 20(2023). [2] Y. Guo, IEEE Electron Device Lett. **46**, 556(2025). [3] P. Sharma, Appl. Phys. Lett. **125**, 253502(2024). [4] D. Chettri, Appl. Phys. Lett. **125**, 202104(2024). [5] Y. Qin, IEEE Electron Device Lett. **47**, 245(2026).

12:05pm **IWGO-FrM2-50 Closing Remarks**

Author Index

Bold page numbers indicate presenter