International Workshop on Gallium Oxide and Related Materials (IWGO-6)
Room ESJ 0202 - Session IWGO-TuA2

Defects Science III & Thermal Management

Moderators: Martin Kuball, University of Bristol, **Heather Splawn**, KYMA TECHNOLOGIES, INC.

3:55pm **IWGO-TuA2-24 Conductive Al_2O_3 with Ohmic Contacts via Ion Implantation***, **Alan Jacobs**, Katie Gann, James Lundh, Daniel Pennachio, Darshana Wickramaratne, Karl Hobart, Michael Mastro,* Naval Research Laboratory

Interest in β-Ga_2O_3 and β-$Al_xGa_{(2-x)}O_3$ has been driven by both the ultra-wide bandgap, enabling step-change improvements in device figures of merit, as well as the availability and scalability of melt-grown oxide substrates. Recent interest has extended this regime into α-$Al_xGa_{(2-x)}O_3$ for bandgap tunability toward the ultimate potential of α-Al_2O_3 at nearly 9eV. Here we report on generation of conductive Al_2O_3 via ion implantation with ohmic contacts and low thermal activation energy of resistivity suggesting a shallow dopant or impurity band conduction.

Conductive α-Al_2O_3 has been previously reported with silicon doping by both ion implantation and growth by MBE[1-2]. Reported as-grown conductivity was minimal but increased to ~0.1mA at 100V after annealing at 1400°C. Reports of ion implanted samples exhibited conductivity ~1µA at 100V after annealing at 1300°C, which reduced at higher anneal temperatures.

Here, bulk sapphire wafers were blanket implanted with silicon, or silicon and oxygen at doses of $1.08*10^{15}$ and $1.62*10^{15}$ cm^{-2} respectively, with oxygen intending to maintain stoichiometry. As-implanted, the silicon doped material exhibited a faint coloration by eye while co-implanted material appeared slightly darker. After annealing in N_2 or Ar ambient at 1000°C for 10 minutes, the material darkened, whereas material annealed in vacuum turned transparent. Samples had Ti/Au (20/200nm) contacts with isolation regions formed by Ar/Cl reactive ion etch. Isolation current across a trench remained at the noise floor of ~10 fA up to 10 V.

Linear transmission-line measurements of silicon doped films exhibit sheet and specific contact resistances of 206 kΩ/□ and $3.8*10^{-4}$ Ω cm^{-2} respectively. Films co-doped with both silicon and oxygen were measured at 75.0 kΩ/□ and $7.5e*10^{-5}$ Ω cm^{-2} respectively. Van der Pauw measurements taken at up to 500°C exhibit a low activation energy of ~57 meV. Thermal activation may exhibit two regimes: low temperature (100-400°C) at 49 meV and a high temperature regime (400-500°C) at 90 meV warranting further investigation. Van der Pauw measurements of unimplanted material exhibits no measurable current until high temperatures, exceeding 120 GΩ/□ until ~800°C and exhibiting a high thermal activation energy of ~1.31 eV from 800-950°C. X-ray diffraction shows strain recovery and significant reduction of gross point defect populations after annealing at 1000°C.

[1] Hironori Okumura 2022 *Jpn. J. Appl. Phys.* **61** 125505. DOI: 10.35848/1347-4065/aca196

[2] Hironori Okumura *et al.* 2021 *Jpn. J. Appl. Phys.* **60** 106502. DOI: 10.35848/1347-4065/ac21af

$^{+}$Author for correspondence: alan.g.jacobs3.civ@us.navy.mil

4:10pm **IWGO-TuA2-27 In-Situ X-Ray Topography Observation of Behavior of Dislocations in β-Ga_2O_3(001) Schottky Barrier Diode During Applying Voltage***, **Daiki Katsube**,* Japan Fine Ceramics Center, Japan*; Yongzhao Yao,* Mie University, Japan*; Daiki Wakimoto, Hironobu Miyamoto, Kohei Sasaki, Akito Kuramata,* Novel Crystal Technology, Japan*; Yukari Ishikawa,* Japan Fine Ceramics Center, Japan

In the next-generation power semiconductor β-Ga_2O_3, the impact of dislocations on device performance remains unclear, and understanding dislocation behavior during device operation is a critical issue. In this study, we performed in-situ observation of dislocation behavior in a β-Ga_2O_3(001) Schottky barrier diode (SBD) under applied voltage using in-situ X-ray topography (XRT) technique.

Monochromatic X-rays (11.27 keV, KEK-PF) were used to conduct in-situ XRT observations of a β-Ga_2O_3(001) SBD device during applying voltage. The SBD had a vertical device structure with voltage applied between the surface and backside electrodes. In-situ XRT observations were performed in a reflection geometry from the surface electrode side of the SBD. The diffraction condition g = 316, which enables observation of all in-plane dislocations, was employed.

Figure 1 shows the XRT image of the SBD. To enable reflection XRT observation of dislocations within the device, the surface electrode (region outlined by yellow lines) was fabricated with a thickness of 100 nm, thinner than that of a conventional SBD. In contrast, the electrode pad (indicated by a blue circle) was deposited with a conventional electrode thickness (approximately 1 µm). Voltage was applied to the electrode pad through wiring that appears as black shadow-like lines in the image, connected to the surface electrode. The white and black lines visible in the image correspond to dislocations present in the SBD. During applying voltage, in-situ observation revealed that dislocations moved. Among the dislocations moving, most of them were located near the thin film electrode edge, and moved toward the thin film electrode edge.

4:25pm **IWGO-TuA2-30 Killer Defects in (011) HVPE-Grown β-Ga2O3 Schottky Barrier Diodes Studied by Synchrotron X-ray Topography and Emission Microscopy***, **Masanori Eguchi**,* Synchrotron Light Application Center, Saga University, Japan*; Shotaro Nakaniwa, Makoto Sato, Niloy Chandra Saha,* Department of Electrical and Electronic Engineering, Saga University, Japan*; Chia-Hung Lin, Kohei Sasaki,* Novel Crystal Technology, Japan*; Makoto Kasu,* Department of Electrical and Electronic Engineering, Saga University, Japan

β-gallium oxide (β-Ga_2O_3) possesses an ultra-wide bandgap of 4.8 eV and a high breakdown field of 8 MV/cm. Therefore, it is expected to become a promising material for high-power, highly efficient electronic devices. However, crystal defects, so-called killer defects in β-Ga_2O_3, cause reverse leakage current and lower off-state breakdown voltage in Schottky barrier diodes (SBDs). The (011) surface was reported to exhibit lower defect density than the (001) surface. Therefore, in this study, we elucidate the killer defects in (011)β-Ga_2O_3 SBDs and find that microcracks along the [100] direction are killer defects.

4:40pm **IWGO-TuA2-33 Impact of Bias Dependent Joule Heating on Gallium Oxide Lateral Transistors via Deep UV Thermal Imaging***, **Dominic Myren**,* University of Connecticut*; Daniel Dryden,* Air Force Research Laboratory*; Cameron Gorsak, Hari Nair,* Cornell University*; Ahmad Islam, Andrew Green,* Air Force Research Laboratory*; Georges Pavlidis,* University of Connecticut

As Gallium Oxide (Ga_2O_3) lateral transistors are advanced toward high-voltage and high-power switching regimes, self-heating driven by bias-dependent Joule dissipation emerges as a critical limitation to performance and reliability. In contrast to established Gallium Nitride technology, the relatively low thermal conductivity of Ga_2O_3 exacerbates localized thermal accumulation, particularly under non-uniform electric field distributions. This work experimentally investigates the impact of bias conditions on the Joule heating profile in lateral Ga_2O_3 transistors [1] and captures the transient evolution of thermal hotspots across operational regimes relevant to high power electronics.

Direct mapping of the Ga_2O_3 channel temperature is not trivial when leveraging traditional methods for thermal characterization.[2] Due to its inherent wide band gap (≈ 4.6 eV), optical techniques require probing wavelengths in the Deep Ultraviolet (DUV) range to directly measure the surface temperature. Any sub-bandgap excitation will result in depth averaged temperature measurements that extend into the Gallium oxide substrate and underpredict the peak temperature. While nanoparticle Raman thermometry can overcome this challenge, it is a point measurement which features low throughput for channel thermal mapping. This study presents a newly developed DUV wide field thermoreflectance imaging microscope that can transmit wavelengths down to 260 nm with sub-micron spatial resolution and a 50× objective.

The gate voltage is varied from partially depletion (-3.5 V) to fully open channel conditions (0 V). In parallel, the drain voltage is adjusted to match the same average power density across the device. Pronounced thermal confinement is observed near the gate (56% elevated peak temperature rise when increasing the drain voltage from 10 to 21.5 V). These findings establish a direct correlation between bias-dependent electric field profiles and transient thermal behavior in gallium oxide devices. The study underscores the necessity of incorporating electro-thermal co-design strategies, including field management and device geometry optimization, to mitigate localized overheating. Deep UV thermal imaging proves to be a powerful diagnostic tool for resolving nanoscale thermal phenomena in ultra-wide bandgap semiconductors, providing critical insight into reliability challenges as gallium oxide transistors are scaled toward next-generation high-power applications. [1] D. M. Dryden et al., APL Electronic Devices 2, 026108 (2026) [2] D. Myren et al., Appl. Phys. Lett. **126**, 200502 (2025).

4:55pm **IWGO-TuA2-36 Engineered Substrates for Ga_2O_3 Vertical Power Devices**, ***Caroline Reilly,*** Kyma Technologies, Inc.*; Sean O'Leary,* Modern Microsystems, Inc.*; Emma Rocco,* US Naval Research Laboratory*; Craig McGray,* Modern Microsystems, Inc.*; Marko Tadjer, Karl Hobart,* US Naval Research Laboratory*; Heather Splawn, Jacob Leach,* Kyma Technologies, Inc.

The ability of Ga_2O_3 to handle thermal loads has been questioned due to its relatively low thermal conductivity. While it has yet to be seen what thermal problems arise in high voltage power switching applications, parallel efforts to mitigate this risk include packaging solutions and approaches such as engineered substrates. Engineered substrates have been developed for other semiconductors (i.e. SOI, QST™, SmartSiC™) and provide performance and/or supply chain benefits over bulk substrates. In the case of Ga_2O_3, using SiC as an underlying carrier wafer could reduce substrate thermal resistance by 50x. While efforts have shown the feasibility of Ga_2O_3-SiC composite wafers, this work seeks to prepare Ga_2O_3-SiC composite wafers for high voltage vertical Ga_2O_3 devices. Beyond the primary goal of a thermally conductive substrate, this application necessitates additional considerations towards interface electrical conductivity and the ability to grow Ga_2O_3 on the engineered substrate.

Bonding of 2” Ga_2O_3 to n-type 100mm SiC has been conducted utilizing interlayers expected to be both thermally and electrically conductive, such as n-Si, TiN_x, and ITO. As-bonded wafers have shown areal yields of >80%, with thinned composite wafers having 60% or greater areal yields. Polished composite wafer coupons have been prepared with remaining Ga_2O_3 thicknesses ~2µm and surface roughness <1 nm. Interface thermal resistances of ~23 m^2K/GW have been measured, such that the interface provides a negligible thermal barrier. Electrical conductivity measurements through full-thickness bonded Ga_2O_3-SiC wafers indicate that ITO is a promising interlayer, providing significantly less resistance than alternatives. Initial growth results on composite wafers have produced layers with similar roughness as those grown on bulk Ga_2O_3. More details on the composite wafer preparation, electrical and thermal conductivity, and growth results will be presented at the conference.

Acknowledgements

This technology was primarily supported by the Microelectronics Commons Program, a DoW initiative, under award number N00164-23-9-G059. The funders had no role in study design, data collection or analysis, or preparation of the manuscript.

Author Index

Bold page numbers indicate presenter