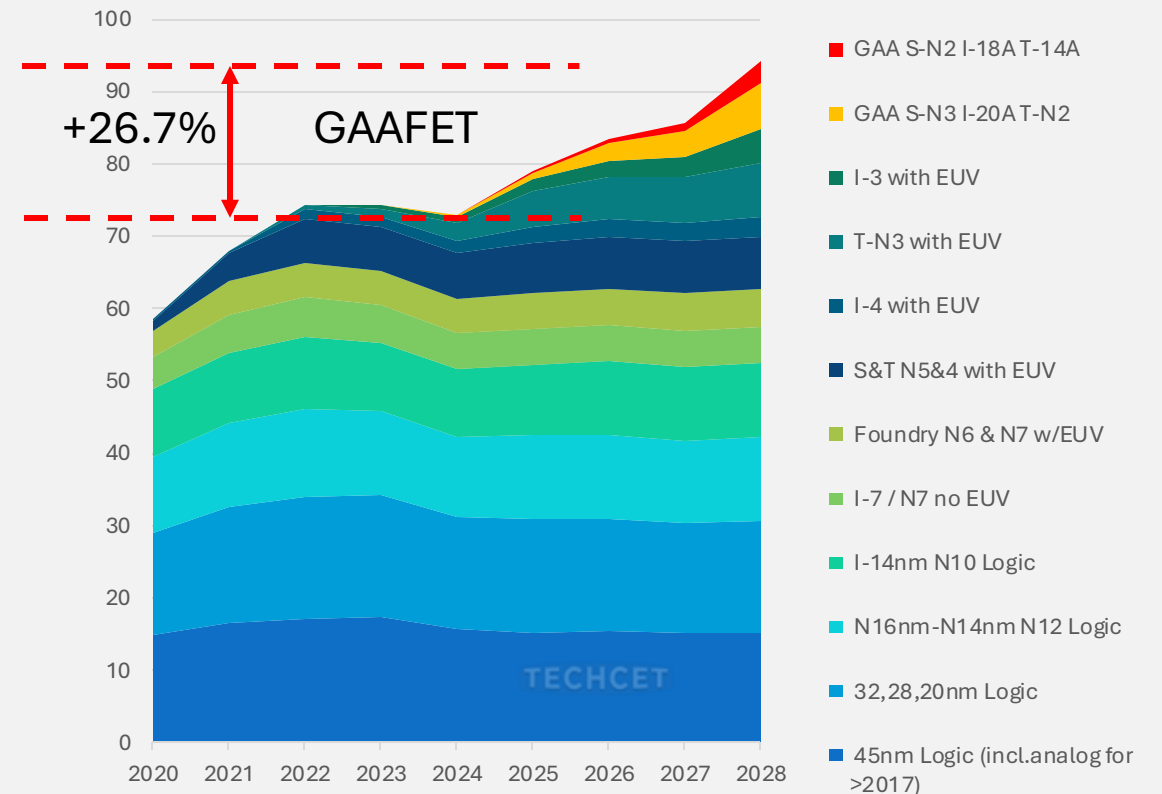


LEADING NODES FORECASTED TO SEE 26.7% GROWTH IN WAFER STARTS BY 2028, DRIVEN BY GAA-FET, PATTERNING AND ADVANCED PRECURSOR INNOVATIONS

Increased Demand for Advanced Deposition Techniques: As leading-edge nodes move towards sub-2nm technology, the need for precision deposition processes such as PEALD (Plasma-Enhanced Atomic Layer Deposition) and advanced CVD techniques is expected to grow. These methods are critical to ensuring uniform layer deposition and supporting the high-performance requirements of GAA-FET and other next-generation architectures.

- Forecasted 26.7% growth 2023 to 2028 in wafer starts expected for Leading nodes with ALD and advanced CVD precursors.
- Starting now GAA-FET new transistor architecture for 2 nm and below, will drive additional growth with new applications in metallization and Epi stack
- According to ASMI the combined CVD and ALD opportunity is 40% higher for GAAFET than FinFET transistor architecture. Therefore, CVD and ALD precursor demand for leading edge will accelerate starting 2025 due to both demand and more wafer passes for CVD and ALD at the leading Foundries TSMC, Samsung, Intel and Rapidus (2027)
- Mutli-patterning bs SADP and SAQP will remain in use for all nodes continuously requiring PEALD dielectric precursors and new innovations, especially for the transition to EUV double patterning

*Leading Edge Logic Wafer Start Forecast 45 to 1.4 nm
(Million 200 mm Wafer Eq.)*



Source: TECHCET CALLC