Functional Thin Films and Surfaces
Room Palm 5-6 - Session MB2-2-MoA

Thin Films for Electronic Devices II

Moderators: Spyros Kassavetis, Aristotle University of Thessaloniki, Greece, **Tomas Kubart**, Uppsala University, Sweden

2:40pm **MB2-2-MoA-4 Polycarbonate Transfer Techniques for the Fabrication of MoS_2 Based Field Effect Transistors***, Chih-Hao Chiang, Ruo-Yao Wang, **Meng-Lin Tsai [g9711566@gmail.com]**,* National Taiwan University of Science and Technology, Taiwan

In recent years, transition metal dichalcogenides (TMDs) have received significant attention due to their immense potential to extend Moore's Law, positioning them as promising semiconductor materials for next-generation electronic devices. The challenges of large-scale production and commercialization of TMDs remain key challenges for future development in practical applications. In the fabrication of TMD-based semiconductor devices, the interface between metal electrodes and TMD layers is critical. Traditional metal electrode deposition techniques facilitate the diffusion of metals in the TMD, potentially reducing the device performance or preventing proper operation. In this study, the metal electrode transfer technique using polycarbonate has been developed to significantly reduce such damage, ensuring the reliable operation of semiconductor devices. Gold electrodes initially deposited on silicon or SiO_2/Si substrates via metal mask (channel length of 20 μm) and photolithography (channel lengths of 8 μm for photodetectors and 3 μm for field-effect transistors, FETs) have been successfully onto chemical vapor deposition (CVD)-grown MoS_2 nanosheets. The as-fabricated field effect transistors (FETs) have been characterized to exhibit switching current ratios of approximately 10^4.

3:00pm **MB2-2-MoA-5 Advancing Piezo-Gated Transistor Performance by Bilayer of V-doped ZnO and Mesoporous PVDF-TrFE***, **Yu Zhen Zhang [n56124650@gs.ncku.edu.tw]**,* National Cheng Kung University (NCKU), Taiwan

In recent years, technology has rapidly advanced, enabling the development of flexible wearable electronics with great potential for applications such as nanogenerators and pressure sensors. Among flexible materials, β-phase PVDF-TrFE, which exhibits piezoelectric properties (d_{33}=30–40pC/N), stands out as a promising composite. This polymer has a semicrystalline structure and displays excellent piezoelectric and ferroelectric properties while maintaining flexibility. However, VZO (d_{33}=12–22pC/N) is also a piezoelectric material, and we aim to improve the device output by depositing it on PVDF-TrFE.

In this study, we aimed to enhance the flexibility and piezoelectric performance of PVDF-TrFE by blending it with zinc oxide nanoparticles and subjecting the mixture to thermal annealing at 120°C. We then applied 11,000 V through corona poling to align the dipole directions within the composite, followed by etching the ZnO to create a porous structure. Additionally, we used radio frequency magnetron co-sputtering that uses ZnO and V_2O_5 as targets to deposit VZO thin film on both sides of the PVDF-TrFE to serve as conduction pathways. Finally, we deposited two Au electrodes to make a piezoelectric gate transistor device.

In the XRD analysis, we examined unpoled and corona-poled samples. The XRD patterns of the unpoled sample showed two peaks corresponding to the α phase which has negatively affects the piezoelectric properties. After poling, the pattern of the poled sample confirmed that the β phase completely dominates the PVDF-TrFE.

We investigated the current output of the piezoelectric gate transistor under various mechanical stresses at a 1V bias and 1Hz frequency. Devices with different dipole orientations exhibited opposite behaviors. Applying mechanical stress to the positively polarized surface generated negative charges at the VZO and PVDF-TrFE interface, creating a depletion region in the top surface channel and reducing current. Conversely, this led to an accumulation region, enhancing current. By applying a piezoelectric field to the gate, we could adjust the semiconductor channel's resistance and control current flow. This technique significantly advances the piezoelectric gate transistor device, paving the way for advanced applications in flexible and wearable electronics and sensing technologies.

4:00pm **MB2-2-MoA-8 Multicomponent Doping for Suppressing Resistivity Scaling of RuAl Intermetallic Compound for Next-Generation Interconnects***, **Yi-Ying Fang [ian6325508428@gmail.com]**, Yung-Hsuan Tsai, Yu-Lin Chen, Shou-Yi Chang,* National Tsing Hua University, Taiwan

Ruthenium (Ru) and molybdenum (Mo) with a low product of resistivity (ρ_0) and electron mean free path (λ) have been considered as potential interconnect materials to replace copper (Cu) [1]. However, as the size of interconnects shrinks, metallic materials with an even shorter λ are needed to suppress resistivity scaling. Intermetallic compounds (IMCs) with strong bonding, a low diffusivity and a short λ, are promising candidates [2]. Previously, we investigated RuAl IMC, which has a low bulk resistivity (14 μΩ-cm), a short λ (about 4 nm) and an excellent thermal stability, but its $\rho_0 \times \lambda$ value (5.6×10^{-16} Ωm^2) is still high, causing a sharp increase in resistivity below 5 nm [3]. This study further added 10% one-to-multicomponent alloys (denoted as 1B-5B) into RuAl B2 IMC using co-sputtering, as a strategy to further reduce λ through lattice distortion and enhanced orbital overlap. Experimental results indicated that the $Al_5Ru_4(nB)_1$ films retained an ordered B2 structure. Electrical measurements revealed that the bulk resistivity was influenced by both the lattice distortion of the IMCs and the electronegativity of the doped elements, which increased the electronic disorder and broadened the band structure [4], leading to a stronger impurity scattering. Although the $Al_5Ru_4(nB)_1$ IMCs had a higher intrinsic resistivity than RuAl, the multicomponent doping effectively reduced the electron mean free path from about 3 nm to only about 1 nm. Consequently, compared to RuAl, the 4B- and 5B-doped $Al_5Ru_4(nB)_1$ IMCs demonstrated a lower $\rho_0 \times \lambda$ value of 4.5×10^{-16} Ωm^2 that is expected to mitigate the sharp resistivity increase at a reduced thickness. Furthermore, the thermal coefficients of resistivity (TCR) of the $Al_5Ru_4(nB)_1$ IMCs of only 0.03/°C were comparable to that of RuAl and lower than that of pure metals, effectively minimizing the resistivity fluctuations with temperature. Additionally, with a large negative formation enthalpy of about -45 kJ/mol, the $Al_5Ru_4(nB)_1$ IMCs exhibited exceptional thermal stability even at an extreme temperature of 800°C, demonstrating its strong potential as a reliable interconnect metallization material without the need of diffusion barrier.

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4:20pm **MB2-2-MoA-9 Fabrication of IZO/IGZO-Based Vertical Thin-Film Transistor and Its Integration with OLEDs for High-Density Display***, **Nahyun Kim [knhangle0215@naver.com]**, Seok Hee Hong, Jun Hyeok Lee, Ho Jin Lee, Tae Geun Kim,* Korea University, Republic of Korea

The rising demand for next-generation applications, such as augmented reality (AR), virtual reality (VR), and wearable devices, has made ultra-high-resolution displays with pixel densities reaching thousands of pixels per inch (PPI) essential. Achieving such high resolutions requires innovative driving circuits and advanced structures for the driving units. Conventional planar thin-film transistors (TFTs) face significant challenges at nanoscale channel lengths, including short-channel effects and threshold voltage (V_{th}) instability, which reduce reliability and performance [1]. Therefore, planar TFTs are inadequate as drivers for high-resolution displays, positioning vertical channel TFTs (VTFTs) as a promising alternative [2]. Conventional VTFTs feature spacers between the top and bottom electrodes, with a channel layer formed along the spacer sidewalls. However, sidewall interface conditions can result in unstable channel characteristics and lower carrier mobility compared to planar TFTs [3],[4].

Herein, we propose a novel VTFT architecture utilizing a dual-layer metal oxide channel structure, as depicted in Figure 1(a). To further enhance integration, the top electrode of the VTFT is employed as the reflective electrode in OLED devices, enabling a VTFT-based top-emitting OLED integration. We address channel stability by implementing an HfO_X-based dual-layer oxide spacer, which generates a quasi-2D electron gas at the oxide interfaces with high electron density, as shown in Figure 1(b). This concentrated electron layer facilitates main channel formation at the interface while optimizing the dual-layer thickness maximizes carrier mobility along the channel path. Additionally, pulsed Joule heating enables localized activation of the active layer without external thermal processing, allowing low-temperature processing by avoiding direct substrate heating. This supports flexible display applications compatible with various substrate materials. Experimental results indicate high performance with a mobility of 16.34 cm^2/Vs, V_{th} of 0.2 V, subthreshold swing of 0.4 V/dec, and an on/off ratio exceeding 10^5 (Figure 1(c)).

Finally, based on these results, we propose an integrated VTFT/OLED structure, realizing a high-integration display component. The integrated VTFT/OLED solution not only offers superior mobility and stability but also supports low-temperature processing for diverse substrates, contributing significantly to advancements in next-generation display technologies. This approach shows substantial potential for applications in AR/VR, wearable devices, and high-resolution monitors, advancing new possibilities in display technology.

4:40pm **MB2-2-MoA-10 Preventing Native Oxide Formation in Niobium Thin Films Through Platinum Encapsulation***, **Ananya Chattaraj [achattara@bnl.gov]**, Aswin Anbalagan,* Brookhaven National Laboratory, USA*; Jinhyun Cho,* Stony Brook University, USA*; Mingzhao Liu,* Brookhaven National Laboratory, USA

This study investigates the impact of encapsulating niobium (Nb) thin films with platinum (Pt) to enhance the performance and stability of qubits in quantum computing, focusing on the role of thin film technology. Niobium-based qubits hold significant promise for quantum computing, but their performance is often compromised by oxide formation and dielectric losses, which contribute to decoherence and limit their coherence times. To address these challenges, a Pt capping layer was applied to Nb thin films with the goal of preventing oxide formation, reducing dielectric loss, and maintaining the superconducting properties of Nb. The Nb thin films were optimized using sputtered deposition, ensuring high-quality film growth, and Pt was subsequently deposited in a controlled, oxygen-free environment to minimize exposure to the atmosphere and reduce the risk of oxidation. To evaluate the effectiveness of the Pt encapsulation, a series of structural and chemical analyses were conducted, including Grazing Incidence X-ray Diffraction, and Hard X-ray Photoelectron Spectroscopy. These techniques confirmed that the Pt capping layer effectively prevented the formation of significant oxide layers at the Nb/Pt interface, an essential factor in improving qubit stability and mitigating decoherence. While some alloying between Nb and Pt was observed, it did not negatively impact the superconducting properties of the Nb films, which maintained a critical transition temperature (Tc) of approximately 9 K. This indicates that the superconductivity of Nb was preserved despite the Pt encapsulation, highlighting the potential of this approach to enhance qubit stability without compromising performance. The results demonstrate that encapsulating Nb with Pt in thin film form significantly improves qubit stability by mitigating dielectric loss and oxide formation, crucial factors for maintaining coherence in quantum computing. This method offers a promising pathway for improving the performance of Nb-based qubits, particularly in applications such as quantum communication, where long coherence times and stable qubits are vital for efficient data processing and analysis. While the results are promising, further research is needed to refine deposition techniques, explore alternative capping materials, and optimize the fabrication process to achieve even longer coherence times. These efforts are essential to realizing the full potential of Nb-based qubits in practical quantum computing applications.

References

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