Electronic and Photonic Devices, Circuits and Applications
Room Davis Hall 101 - Session EP+HM+MD-MoA

Processes/Devices I
Moderator: Yuhao Zhang, Virginia Tech

1:45pm **EP+HM+MD-MoA-1 Gallium Oxide – Heterogenous Integration with Diamond for Advanced Device Structures**, *H. Kim, A. Bhat, A. Nandi, V. Charan, I. Sanyal, A. Mishra, Z. Abdallah, M. Smith, J. Pomeroy, D. Cherns,* ***Martin Kuball,*** University of Bristol, UK **INVITED**

Potentials for heterogenous integration of Ga_2O_3 with high thermal conductivity materials such as diamond for enabling energy-efficient kV-class power devices are being discussed. The integration alleviates Ga_2O_3 material drawbacks such as its low thermal conductivity and inefficient hole conductivity. The benefits of heterogeneous integration are for example demonstrated through electrical and thermal simulations of a Ga_2O_3-Al_2O_3-diamond superjunction based Schottky barrier diode. The simulation studies show that the novel device has potential to break the R_{ON}-breakdown voltage limit of Ga_2O_3, while showing relatively low rise in temperature compared to conventional devices. As step into their realization, experimental Al_2O_3 assessment namely ledge features in the capacitance-voltage (CV) profiles of Ga_2O_3 metal-oxide-semiconductor (MOS) capacitors were investigated using UV-assisted CV measurements; an interface trapping model is presented whereby the capacitance ledge is associated with carrier trapping in deep-level states at the Al_2O_3/Ga_2O_3 interface. Trench-Schottky Barrier diodes with breakdown voltage in excess of 1.5kV were demonstrated. First steps for the materials integration of Ga_2O_3 with diamond towards a superjunction based trench-Schottky barrier diode, including epitaxial growth of Ga_2O_3 on single crystal diamond substrates are being reported.

2:15pm **EP+HM+MD-MoA-3 Highly Scaled β-Ga2O3 MOSFET with 5.4 MV/cm Average Breakdown Field and Near 50 GHz fMAX**, ***Chinmoy Nath Saha,*** *A. vaidya,* SUNY at Buffalo*; A. Bhuiyan, L. Meng,* Ohio State University*; S. Sharma,* SUNY at Buffalo*; H. Zhao,* Ohio State University*; U. Singisetti,* SUNY at Buffalo

This letter reports the high performance β-Ga2O3 thin channel MOSFET with T gate and degenerately doped source/drain contacts regrown by Metal Organic Chemical Vapour Deposition (MOCVD). Device epitaxial layer was grown by Ozone MBE. Highly scaled T-gate (LG=160-200 nm) was fabricated to achieve enhanced RF performance and passivated with 200 nm Silicon Nitride (Si3N4). Peak drain current (ID,MAX) of 285 mA/mm and peak trans-conductance (gm) of 52 mS/mm were measured at 10 V drain bias with 23.5 Ω mm on resistance (Ron). Metal/n+ contact resistance of 0.078 Ω mm was extracted from Transfer Length Measurements (TLM). Channel sheet resistance was measured to be 14.2 Kiloohm/square from cross bar structure. Based on TLM and cross bar measurements, we determined that on resistance (Ron) is possibly dominated by interface resistance between channel and regrown layer. Different growth methods originating from MBE channel layer and MOCVD regrown n++ layer can cause this high interface resistance. A gate-to-drain breakdown voltage(V_{DG}) of 192 V is measured for L_{GD}= 355 nm resulting in average breakdown field (E_{AVG}) of 5.4 MV/cm. This $E_{AVG}$is the highest reported among all sub-micron gate length lateral FETs. And highest overall without using any intentional field plate techniques. Current gain cut off frequency (f_T) of 11 GHz and record power gain cut off frequency (f_{MAX}) of approximately 48 GHz were extracted from small signal measurements. f_T is possibly limited by DC-RF dispersion due to interface traps which need further investigation. We observed moderate DC-RF dispersion at 200 ns pulse width (for both output and transfer curve) which can corroborate our theory. We recorded f_T.V_{BR} product of 2.112 THz.V for 192 V breakdown voltage which is similar to GaN HEMT devices. Our device surpasses the switching figure of merit of Silicon because of low on resistance and high breakdown voltage, and competitive with mature wide-band gap devices. Proper surface cleaning between channel and regrowth layer and sub-100 nm T gate device structure can pave the way for better RF performance.

2:30pm **EP+HM+MD-MoA-4 Demonstration of a β-Ga_2O_3 Lateral Diode Full-Wave Rectifier Monolithic Integrated Circuit**, ***Jeremiah Williams,*** *J. Piel, A. Islam, N. Hendricks, D. Dryden, N. Moser,* Air Force Research Laboratory, Sensors Directorate*; W. Wang,* Wright State University*; K. Liddy, M. Ngo,* Air Force Research Laboratory, Sensors Directorate*; N. Sepelak,* KBR Inc.*; A. Green,* Air Force Research Laboratory, Sensors Directorate

Beta Gallium Oxide (Ga_2O_3) is well positioned excel in high power density applications due to its wide band gap, critical field strength, multiple shallow donor species, and melt grown native substrates. Monolithic integrated circuits (ICs) can advance Ga_2O_3 by reducing the size, weight, and connectivity parasitics of components. Lateral topologies with thin epitaxy on insulating substrates enable simple fabrication and integration of RF components. This work utilizes this system to demonstrate a fundamental circuit, the diode full-wave rectifier, with an accompanying design study of the interdigitated lateral diode topology.

The devices (Fig. 1) are fabricated from a 65 nm Si-doped Ga_2O_3 epitaxial layer grown by MBE on a Fe-doped Ga_2O_3 substrate. Epitaxy carrier concentration is measured to be 2×10^{18} cm^{-3} from C-V test structures (Fig. 2). The cathode is a Ti/Al/Ni/Au Ohmic contact annealed at 470 °C. The devices are isolated with a BCl_3 ICP mesa etch. A field-plate and surface passivation oxide of 80 nm thick Al_2O_3 is deposited by ALD. The anode is a Ni/Au Schottky contact. A full-wave rectifier and 16 diode variations are evaluated. The diodes have square and rounded contacts; anode finger counts of 1, 2, 4, and 8; and anode-cathode lengths ($L_{A\text{-}C}$) of 5, 7, and 12 µm. Anode length is 4 µm and width is 48 µm. The diodes in the rectifier have round contacts, 4 anode fingers, and 12 µm $L_{A\text{-}C}$ (Fig. 3). The rectifier is measured on-chip with micro probes. An AC signal is generated with a high-voltage amplifier and measured on an oscilloscope. The output of the rectifier to a 47 kΩ load is measured differentially, using a voltage divider to protect the oscilloscope from voltage spikes (Fig. 4).

The rectifier successfully demonstrates full-wave rectification of sine waves up to 144 V_{rms} (205 V peak) and 400 Hz (Fig. 5). The rectifier demonstrates 83 % efficiency and 0.78 W peak power. To the authors' knowledge, this is the first demonstration of a diode full-waver rectifier IC in Ga_2O_3. From the lateral diode design study, rounded contacts improve the average breakdown voltage (V_{bk}) by 20% (+41 V) without effecting specific on-resistance ($R\text{-}_{on,sp}$) (Fig. 6). The number of anode fingers does not statistically affect V_{bk}, and improves average $R\text{-}_{on,sp}$ by 18% (-0.45 mΩ-cm^2) at eight (Fig. 7). Scaling $L_{A\text{-}C}$ to 5, 7, and 12 µm also scales average $R_{on,sp}$ to 2.0, 2.9, and 8.6 mΩ-cm^2. Average V_{bk} scales as well, but with no change between 5 and 7 µm $L_{A\text{-}C}$ (248, 242, and 341 V) (Fig. 8). The J-V characteristics of a single diode (round contacts, eight fingers, 5 µm $L_{A\text{-}C}$) are included in Fig. 9.

2:45pm **EP+HM+MD-MoA-5 Improved Breakdown Strength of Lateral β-Ga_2O_3 MOSFETs Using Aerosol-Spray-Printed hBN-BCB Composite Encapsulation**, ***Daniel Dryden,*** Air Force Research Laboratory, Sensors Directorate*; L. Davidson,* KBR, Inc.*; K. Liddy, J. Williams, T. Pandhi, A. Islam, N. Hendricks, J. Piel,* Air Force Research Laboratory, Sensors Directorate*; N. Sepelak,* KBR, Inc.*; D. Walker, Jr., K. Leedy,* Air Force Research Laboratory, Sensors Directorate*; T. Asel, S. Mou,* Air Force Research Laboratory, Materials and Manufacturing Directorate, USA*; F. Ouchen,* KBR, Inc.*; E. Heckman, A. Green,* Air Force Research Laboratory, Sensors Directorate

Beta gallium oxide (β-Ga_2O_3) has shown promise for high-voltage power devices and power switching due to its large critical field strength E_c estimated at 8 MV/cm [1]. Dielectric passivation and testing under Fluorinert immersion [2] are used to increase breakdown voltage V_{bk} and avoid air breakdown, respectively, with the highest V_{bk} lateral Ga_2O_3 devices using polymer passivation [3]. The polymer benzocyclobutene (BCB) exhibits high dielectric strength, low parasitics, and good manufacturability [4,5]. It may be loaded with hexagonal boron nitride (hBN), improving thermal conductivity, dielectric response, and mechanical durability [6]. Coatings can be applied via aerosol jet printing, allowing multiple experimental conditions across devices on a single sample. Here, lateral β-Ga_2O_3 MOSFETs encapsulated with hBN-loaded BCB (hBN-BCB) which exhibit significantly enhanced V_{bk} compared to devices encapsulated with BCB alone or without encapsulation.

Si-doped β-Ga_2O_3 was grown epitaxially on a semi-insulating, Fe-doped (010) Ga_2O_3 substrate via molecular beam epitaxy to a nominal thickness of 65 nm and a doping of $2.8\text{+-}0.2\text{x}10^{17}$ cm^{-3}. Ti/Al/Ni/Au ohmic contacts were deposited and annealed at 470 °C for 60 s in N_2. Ni/Au gates were deposited on a gate oxide of 20 nm Al_2O_3, followed by a passivation oxide of 85 nm Al_2O_3. Thick Au contacts were formed using evaporation and electroplating. Devices with BCB or hBN-BCB were encapsulated using an

Optomec AJ200 aerosol jet printer. Inks consisted of Cyclotene 4022-35, cyclohexanone and terpineol, with or without hBN.

V_{bk} was tested under air or Fluorinert (Figure 2). Devices tested under Fluorinert, BCB, and BCB plus Fluorinert showed a 1.7x improvement in V_{bk} over air. Devices with hBN-BCB showed an improvement of 3.7x over air and 1.35x over BCB alone. The hBN-BCB-coated devices (N=6) show significant improvement in V_{bk} over the devices coated BCB alone (N=3) with p<0.011 (single-tail heteroscedastic T-Test).

Device performance of the highest-V_{bk} device are shown in Figure 3. The device, before encapsulation, had R_{on} of 683 Ω·mm, I_{max} of 3.42 mA/mm, $G_{m,peak}$ of 1.14 mS/mm, V_{th} of -3.8 V, V_{off} of -6.5 V, and V_{bk} of 951 V ($E_{crit,avg}$ 1.23 MV/cm). Device performance was unaffected by hBN-BCB encapsulation (Fig. 3b) excepting a change in V_{off} to -8 V. No significant gate leakage was observed during device operation or breakdown. Breakdown likely occurred due to peak fields exceeding the E_{crit} of one or more materials at the drain-side edge of the gate. These results provide a significant improvement over existing encapsulation approaches in β-Ga_2O_3 lateral MOSFETs.

3:00pm **EP+HM+MD-MoA-6 Wafer-Scale β-Ga_2O_3 Field Effect Transistors with MOCVD-Grown Channel Layers**, ***Carl Peterson***, University of California Santa Barbara*; F. Alema,* Agnitron Technology Incorporated*; Z. Ling, A. Bhattacharyya,* University of California Santa Barbara*; S. Roy,* University of California at Santa Barbara*; A. Osinsky,* Agnitron Technology Incorporated*; S. Krishnamoorthy,* University of California Santa Barbara

We report on the growth, fabrication, and wafer-scale characterization of lateral high-voltage MOSFETs with ~120-160 mA/mm on current on a large area 1" Synoptics™ insulating substrate. A ~170nm Si-doped β-Ga_2O_3 channel with an electron concentration of ~3 x 10^{17} cm^{-3} was grown via metalorganic chemical vapor deposition (MOCVD) on a 1" Fe-doped (010) bulk substrate which was subjected to a 30min HF treatment prior to growth. The growth was done using Agnitron Technology's Agilis 700 MOVPE reactor with TEGa, O_2, and Disilane (Si_2H_6) as precursors with Ar as the carrier gas. A ~210nm unintentionally doped (UID) buffer layer was grown on top of the substrate. The source and drain ohmic contacts were selectively regrown and patterned with a BCl_3 Reactive Ion Etch (RIE) and HCl wet clean. n^+ β-Ga_2O_3 was then grown via MOCVD using Silane (SiH_4) as the silicon precursor and a Ti/Au/Ni Ohmic metal stack was deposited on the regrown regions. A 30nm Al_2O_3 gate dielectric was deposited via ALD at 300C. Lastly, a Ni/Au/Ni gate metal was deposited. The channel sheet charge was measured to be uniform across the wafer (4.6 x 10^{12} cm^{-2} ± 0.6 x 10^{12} cm^{-2}), estimated from the MOSCAP C-V characterization (V_{GS} of +10V (accumulation) to pinch-off). The output and transfer characteristics were measured across the wafer for devices with 1/1.5/1 µm $L_{GS}/L_G/L_{GD}$ dimensions. The pinch-off voltage had a large variation across the wafer (-30 ± 15V). The apparent charge profile from the C-V curves indicates the presence of a parasitic channel at the substrate-epilayer interface which is distributed non-uniformly across the wafer. The on-current (I_D) measured across the wafer was more uniform about 140 ± 20 mA/mm (V_{GS} = +10 V, V_{DS} = 15 V). CV measurements and transfer characteristics indicate a significant density of slow traps (negatively charged) at the dielectric/semiconductor interface, leading to a repeatable shift in the transfer curve from the 2nd scan onward. The MOSFET devices were measured without any field plating or passivation in Fluorinert and the three-terminal destructive breakdown voltages for 5µm and 20µm L_{GD} were 0.65 and 2.1 kV, respectively. Demonstration of wafer-scale growth, processing, and characterization of MOSFETs on a domestic bulk substrate platform reported here is a key step highlighting the technological potential of beta-Gallium Oxide. Acknowledgments: We acknowledge funding from II-VI Foundation, UES Inc. and discussions with AFRL.

3:15pm **EP+HM+MD-MoA-7 Modelling of Impedance Dispersion in Lateral β-Ga_2O_3 MOSFETs Due to Parallel Conductive Si-Accumulation Layer**, ***Zequan Chen***, *A. Mishra, A. Bhat, M. Smith, M. Uren,* University of Bristol, UK*; S. Kumar, M. Higashiwaki,* National Institute of Information and Communications Technology, Japan*; M. Kuball,* University of Bristol, UK

Off-state leakage currents in lateral β-Ga_2O_3 FET devices have previously been attributed to the presence of unintentional Si (n-type) at the interface between epitaxial layer and the substrate[1-5], i.e. a parallel leakage conducting channel. Fe-doping (>$10^{19}$$cm^{-3}$) near the surface of the β-Ga_2O_3 substrate, followed by thermal annealing, has been proven to compensate the unintentional Si impurities, to some degree, thereby reducing leakage current in devices; however, elevated off-state currents and low on-off ratios are still observed in these devices[5]. This work is to provide an analytical model to describe the observed device frequency dispersion due to parallel conductive Si-accumulation layers. Particularly, the dispersion is not associated with active traps as generally believed[6-8].

Lateral β-Ga_2O_3 transistors here were processed on a MBE-grown epitaxial layer on Fe-surface-implanted semi-insulating β-Ga_2O_3 substrates, followed by thermal annealing[5](Fig.1). The transfer characteristics of the device (Fig.2) reveals a large off-state leakage drain current (10^{-6}A/mm) and a small gate leakage current (10^{-12}A/mm). The gate-source capacitance-voltage (C_{GS}) and equivalent conductance-voltage (G_{GS}) profiles between 1kHz and 1MHz (Fig.3) reveal a background dispersion with frequency that is nearly independent of applied gate bias.

An equivalent circuit model is built for explaining impedance dispersion (Fig.4). The parallel leakage path along the entire UID/substrate interface due to Si contaminants provides a coupling path between channels and the probe pads, which are included in the analysis of the device. Therefore, the total capacitance (C_{GS}) will be the "ideal" capacitance (C_{ideal}) superimposed by the contributions from the capacitance and resistance underneath the gate pad(C_{GP}, R_1, C_1), the resistance of the parallel leakage path (R_s), and the capacitance and resistance under the channel (R_2, C_2). Utilizing this model, the measured C_{GS} and G_{GS} are well fitted (Fig.5). The exclusion of traps in the model indicates parallel coupling, instead of traps, should predominantly account for observed frequency dispersion. Moreover, from the extracted R_s in Table.1, the Si concentration at epi/substrate interface is estimated around 1×$10^{18}$$cm^{-3}$, which agrees with that measured from SIMS (Fig.1). This work provides an understanding of the electrical impact of the parallel leakage path of β-Ga_2O_3 devices at moderate frequencies. The signal generated by the parallel leakage can mislead impedance measurements, affecting further analysis such as D_{it} extraction in β-Ga_2O_3 MOSFETs.

Material and Device Processing and Fabrication Techniques
Room Bansal Atrium - Session MD-MoP

Material and Device Processing and Fabrication Techniques
Poster Session I

MD-MoP-2 Characteristics of n-ITO/Ti/Au Multilayer for Ohmic Contact on β-Ga_2O_3 Epitaxial Layer, ***Yusup Jung***, *H. Kim, S. Kim,* Powercubesemi Inc., Republic of Korea*; Y. Jung, D. Chun,* Hyundai Motor Company, Republic of Korea*; T. Kang, S. Kyoung,* Powercubesemi Inc., Republic of Korea

In this paper, The n-ITO/Ti/Au Multilayer for forming an ohmic contact was deposited on the β-Ga_2O_3epitaxial layer by using magnetron sputtering system to apply the source and drain of the lateral β-Ga_2O_3transistor. Multilayer was heated by using Rapid Thermal Annealing (RTA) equipment after deposited multilayer, and the contact resistance, sheet resistance, and linear dependence characteristics were evaluated after measuring the I-V curve using the TLM method. The n-ITO is a transparent conductive material with a band gap of about 3.5eV [1]. It is deposited between β-Ga_2O_3 and Ti metal to improve band alignment between β-$Ga_2O_3$and Ti and to be as an electron injection layer to improve ohmic contact characteristics [2,3]. The n-ITO/Ti/Au Multilayer is deposited on β-Ga_2O_3 epitaxial layer by using DC/RF magnetron sputtering equipment. After deposition process, post annealing process was proceeded within the range of 500 to 800 degrees in a nitrogen gas atmosphere. The I-V characteristics of the fabricated TLM pattern were measured with a keithley 2410. As a result, when the thicknesses of n-ITO, Ti and Au metal were 20nm, 50 nm, and 100 nm, the specific contact resistivity is 1.3 mΩ.cm^2 and exhited strong linear dependence curve at post annealing temperature of 700 degrees.

[Reference]

[1] S.J. Kim, IEEE Photonic Tech L 17, (2005) 1617

[2] J.H Bae, H.Y. Kim, and J.H Kim, ECS J. Solid State Sci. Technol.6, (2017) Q3045

[3] Patrick H. Carey IV, F. Ren, David C. Hays, B.P Gila, S.J. Pearton, S.H. Jang, A. Kuramata, Appl. Surf. Sci 422 (2017) 179

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MD-MoP-3 β-Ga_2O_3 Schottky and Heterojunction Diodes Operating at Temperatures Up to 600°C, ***Kingsley Egbo***, *S. Schaefer, W. Callahan, B. Tellekamp, A. Zakutayev,* National Renewable Energy Laboratory

Semiconductor device performance and reliability under extreme conditions are essential for several applications in the industrial, energy, and automotive sectors. Wide bandgap oxides such as β-Ga_2O_3 are important materials for high-power device applications and are also well-suited for high-temperature electronics due to reduced temperature-activated parasitic leakage and resistance to oxidation.

Here, we explore the high-temperature operation of Ga_2O_3 based Schottky and *p-n* junction diodes. Vertical heterojunction NiO/*β*-Ga_2O_3 diodes and Ni/*β*-Ga_2O_3 Schottky diodes were fabricated and studied using current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements in the range of 25 – 600 °C. For the *p-n* diode, a 200nm thick NiO film was grown on a Sn-doped *β*-Ga_2O_3 (100) substrate (≈2x10^{18} cm^{-3}) by pulsed laser deposition, where the (100) substrate face is effective at promoting (100)-textured NiO. After NiO deposition, the device area was mesa isolated by argon dry etching.[1] The Schottky diode was fabricated on a 300 nm unintentionally doped (UID) layer grown on Sn-doped Ga_2O_3 (001) substrates by molecular beam epitaxy (MBE).[2] Schottky diodes were formed by depositing 30 nm Ni / 100 nm Au via e-beam evaporation. For both types of devices, a stable Ohmic back contact to Ga_2O_3 was formed by 5 nm Ti / 100 nm Au annealed under N_2 at 550 °C for 90 seconds.[3]

In the Schottky diode, the turn-on voltage and rectification ratio were found to be 1.2V and 10^8 (±2V), respectively, at room temperature. The rectification ratio decreased strongly with increasing operating temperature to ≈ 10^2 at 600 °C. The temperature dependence of the on-state voltage and increasing leakage current are attributed to barrier inhomogeneity and instability at Ni/*β*-Ga_2O_3 interface and low built-in potential at the Schottky barrier (≈1.0 eV measured by *C-V*). The NiO/*β*-Ga_2O_3 diodes turn-on voltage at RT was found to be 1.9V. Compared to the Schottky diode, a similar rectification ratio of the order of 10^8 was obtained at RT however the rectification ratio only decreased to ≈10^4 at 600 °C. The NiO heterojunction diode also showed lower reverse leakage current up to -10V compared to the Ni-based Schottky diode at high temperatures. These results suggest that while Ga_2O_3 based Schottky barrier diodes hold some potential for high-temperature operation, they are more fundamentally limited by thermally driven leakage current increases. We show that heterojunction *p-n* diodes can significantly improve high-temperature electronic device and sensor performance due to a higher built-in voltage and favorable band offsets.

MD-MoP-4 Structural Properties of Ga_2O_3 Surfaces Treated by Nitrogen Radical Irradiation, ***Kura Nakaoka***, *S. Taniguchi, T. Kitada, M. Higashiwaki,* Department of Physics and Electronics, Osaka Metropolitan University, Japan

Recently, we found that nitrogen (N) radical irradiation has an effect to significantly restore Ga_2O_3 surface damage and can improve not only Ga_2O_3 Schottky characteristics but also their in-plane uniformity. It can be expected that the nitridation would be one of the key processes for fabrication of various types of Ga_2O_3 devices. In this work, we studied structural properties of nitridated Ga_2O_3 (100) and (010) surfaces to investigate an origin of the improvements in electrical properties.

Surfaces of Ga_2O_3 (100) and (010) substrates were simultaneously nitridated by irradiation of N radicals generated using an RF-plasma cell in a molecular beam epitaxy growth chamber. The process was performed at a substrate temperature of 660℃ for 30, 60, and 120 min. The RF plasma power and N_2 gas flow rate were 500 W and 0.6 sccm, respectively. We observed nitridated Ga_2O_3 surfaces by atomic force microscopy (AFM) and analyzed elemental compositions of the Ga_2O_3 near-surface region using X-ray photoelectron spectroscopy (XPS).

Roughening of the Ga_2O_3 (100) and (010) surfaces occurred by the nitridation process, and the roughness monotonically increased with nitridation time. For the (100) and (010) surfaces, the root-mean-square roughness values were less than 0.2 nm before the N radical irradiation and reached 0.49 and 0.99 nm after the 120-min irradiation, respectively.

Next, we performed XPS analyses for the samples with and without the 120-min N radical irradiation to investigate the progress of nitridation. A clear N 1*s* peak was observed only for the nitridated surfaces, indicating that a large amount of N atoms were successfully incorporated into the Ga_2O_3 by the N radical irradiation. Ga 3*d* peaks of the nitridated surfaces were separated into four gaussian components corresponding to the Ga-O bonding, the Ga-N bonding, the O 2*s* core level, and the N 2*s* core level. The ratios of integrated intensities between the Ga-O and Ga-N peaks, i.e., Ga-N/Ga-O values were 0.51 and 0.74 for the Ga_2O_3 (100) and (010) surfaces, respectively. This result indicates that nitridation more advanced on the (010) surface than the (100) one, which can be attributed to a difference in the density of dangling bonds.

In this study, we investigated structural properties of nitridated Ga_2O_3 (100) and (010) surfaces. Improvements in electrical properties of the Ga_2O_3 Schottky interfaces by N radical treatment are considered due to replacement of a large amount of O atoms by N atoms.

This work was supported in part by the Development Program, “Next-Generation Energy-Saving Devices” of the Ministry of Internal Affairs and Communications, Japan (JPMI00316).

MD-MoP-6 Process Optimization of Sputtered High-K (Sr,Ba,Ca)Tio_3 for Ga_2O_3 Dielectric Layers, ***Bennett Cromer***, *C. Gorsak, W. Zhao, L. Li, H. Nair, J. Hwang, B. Van Dover, D. Jena, G. Xing,* Cornell University

β-Ga_2O_3 provides a unique electrostatic challenge due to its large intrinsic breakdown field of 8 MV/cm and moderate dielectric constant of 10. Maintaining oxide fields near 0.5 MV/cm to minimize leakage and degradation thus requires an oxide ε_r of at least 160. Further, high-k dielectrics such as titanates have significant process-property variation which inhibit process integration. Despite pioneer work on Metal/$BaTiO_3$/β-Ga_2O_3 heterojunction diodes[1] and ($BaTiO_3$/$SrTiO_3$)$_{15}$ high-k field plates[2], key information such as optimal anneal condition and effective dielectric constant at frequency are yet to be explored. In this work, we use metal-insulator-metal (MIM) and co-planar waveguide (CPW) structures to characterize the complex dielectric constant of $BaTiO_3$, $CaTiO_3$, and $SrTiO_3$

thin films from quasistatic to high frequency. By varying parameters such as deposition and anneal temperatures, we identify a desired process window wherein the dielectric constant is large enough to support intrinsic Ga_2O_3 breakdown with minimal leakage current at application-based operating frequencies.

Thin films of $BaTiO_3$, $CaTiO_3$, and $SrTiO_3$ were deposited by RF magnetron sputtering at 25 °C, 350 °C, and 500 °C on HR-Si as test substrates. Deposition conditions were 50 or 100 W bias for 60 minutes at 5 mTorr with 30 sccm gas flow of 9:1 Ar:O_2. Films were characterized by X-Ray diffraction, spectral reflectance, scanning electron microscopy, and atomic force microscopy pre- and post- anneal to assess crystallinity, surface morphology, and grain size if observable. After annealing, MIM and CPW structures were patterned by standard lithography and deposition of Ti/Au contacts. From these structures complex dielectric constant was extracted from measured impedance. Leakage current was captured from DC IV measurements of the MIM structures. The set of process conditions for each high-k dielectric ($BaTiO_3$, $CaTiO_3$, and $SrTiO_3$) which yielded the most promising leakage and dielectric properties was then replicated on vertical field-plated diode and lateral MOSFET test structures and compared directly to low-k and non-field plated structures.

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MD-MoP-7 Electrical Characteristics of MOCVD Grown β-Ga_2O_3 Schottky Diodes on (010) β-Ga_2O_3 Substrates, ***Sudipto Saha,*** University at Buffalo-SUNY*; L. Meng, D. Yu, A. Bhuiyan,* Ohio State University*; H. Zhao,* ohio State University*; U. Singisetti,* University at Buffalo-SUNY

Monoclinic beta-gallium oxide (Ga_2O_3) is a promising material for power electronics and RF switching due to its ultrawide bandgap. Metal-organic chemical vapor deposition (MOCVD) has emerged as a promising technique for growing high-quality Ga_2O_3 films with smooth surface morphology, controllable doping, and high mobility, making it a preferred method for Ga_2O_3 power devices. However, there are limited reports on the fabrication and characterization of vertical power devices using high growth rate MOCVD-grown Ga_2O_3 films, and the performance of Ga_2O_3 vertical power devices has yet to reach its full potential. Vertical Schottky barrier diodes (SBDs) were fabricated on MOCVD-grown Ga_2O_3 films with varying growth rates, showing promising electrical and structural properties for high-power applications.

In this work, three different Si-doped homoepitaxial Ga_2O_3 films were grown on Sn-doped (010) Ga_2O_3 substrates by MOCVD, labeled S1, S2, and S3. The growth rate for S1 is 3 µm/hr, while S2 and S3 have rates of 650 nm/hr. The epilayer thickness for S1, S2, and S3 are 9.5, 3, and 2 µm, respectively. The S1 sample has the roughest surface of the three samples due to its faster growth rate compared to S2 and S3. The Schottky diodes fabricated with the three samples show excellent rectifying behavior. The diode characteristics such as ideality factor, barrier height, and specific on-resistance show an increase with the growth rate and epilayer thickness, as macro and micro-scale surface roughness also increase.At the same growth rate, the sample with a thicker epilayer exhibits lower forward current density and higher leakage current, which can be attributed to the surface roughness. Notably, though the S3 sample exhibits the highest forward current densities (3386 A/cm^2 at 2.5 V) and lowest specific on-resistance (0.707 mΩ.cm^2), S1 exhibits the lowest leakage currents (8.32×10^{-8} A/cm^2 at -2 V), and highest ON-OFF ratios (>10^9). The capacitance-voltage characteristics showed that all three structures have completely depleted Ga_2O_3 layers on the reverse bias side. The extracted doping density of S1, S2, and S3 are 2.02×10^{16}, 1.73×10^{16}, and 6.08×10^{16} cm^{-3}, respectively.

Overall, the fabricated SBDs exhibit promising electrical and structural properties, with a high current rectification ratio and low reverse leakage current, indicating their potential for high-power applications. The results of our study contribute to the understanding of the growth and characterization of MOCVD-grown Ga_2O_3 films and provide valuable insights for developing high-performance power devices based on this promising material.

Advanced Characterization Techniques
Room Davis Hall 101 - Session AC+MD-TuM

Characterization/Modeling IV

Moderator: Baishakhi Mazumder, University of Buffalo, SUNY

10:45am **AC+MD-TuM-10 Defects in Ga_2O_3: An Ultra-high Resolution Electron Microscopy Study**, ***Nasim Alem***, The Pennsylvania State University; *A. Chmielewski,* CEMES-CNRS, France **INVITED**

Interest in β-Ga_2O_3 has dramatically increased in recent years due to the material's potential promise for use in power electronics and extreme environments. Its combination of a monoclinic structure (C2/m space group), two inequivalent tetrahedral and octahedral gallium sites and three inequivalent oxygen sites, and a bandgap of 4.8 eV, 1.4 eV above that of gallium nitride, creates a semiconductor material with a unique set of properties. This is further aided by β-Ga_2O_3's uncommon capability among the ultra-wide bandgap oxides to be grown into high quality single crystal substrates using both melt-based bulk and thin film growth and deposition methods. Defects and their stability and dynamics under static and extreme environments can limit the incorporation of β-Ga_2O_3 into new applications. Therefore, a direct visualization and in-depth understanding of the defects and their interplay with the environment is vital for understanding the materials properties and the device breakdown under extreme conditions. In this presentation we will discuss the atomic, electronic, and chemical structure of the defects in doped and UID β-Ga_2O_3 using scanning transmission electron microscopy (S/TEM) imaging and electron energy loss spectroscopy (EELS). In addition, we will discuss the electronic structure and the local properties in β-Ga_2O_3 under extreme conditions using STEM-EELS. This fundamental understanding is important to uncover the breakdown behavior in β-Ga_2O_3 and the impact of defects on its device performance.

11:15am **AC+MD-TuM-12 Sub-oxide Ga to Enhance Growth Rate of β-Ga_2O_3 by Plasma-assisted Molecular Beam Epitaxy**, ***Zhuoqun Wen***, *K. Khan, E. Ahmadi,* University of Michigan, Ann Arbor

In recent years, there has been significant interest in β-Ga_2O_3 as a potential candidate for the next generation of power electronics, solar-blind ultraviolet (UV) detectors, and as a substrate for UV light emitting diodes (LEDs). This interest stems from its ultra-wide bandgap of 4.8eV. Thin film growth and n-type doping (Si, Sn, Ge) of Ga_2O_3 have been achieved through various methods such as metal-organic chemical vapor deposition (MOCVD), pulsed laser deposition (PLD), and molecular beam epitaxy (MBE). However, MBE has limitations in terms of the growth rate of Ga_2O_3 due to the desorption of volatile Ga_2O, which is formed from the reaction between Ga and Ga_2O_3. Using gallium sub-oxide (Ga_2O) instead of elemental gallium has been previously employed [1] as a technique to enhance the growth rate of Ga_2O_3 by Ozone-MBE. However, this technique has not yet been investigated in plasma-assisted MBE. In my talk, I will present the results of our recent studies on using Ga_2O as Ga source in PAMBE. Using the same plasma conditions, we show that using Ga_2O instead of Ga can at least double the growth rate of Ga_2O_3.

Previously, we have demonstrated uniform and controllable silicon doping of β-Ga_2O_3 by utilizing disilane (Si_2H_6) as the Si source. [2] In my talk, I will show that this technique is also compatible with utilizing Ga_2O as Ga source. The silicon doping can be tuned from 3×10^{16} cm^{-3} to 1×10^{19} cm^{-3} using the diluted disilane source.

References:

1. Vogt, P., Hensling, F. V., Azizie, K., Chang, C. S., Turner, D., Park, J., ... & Schlom, D. G. (2021). Adsorption-controlled growth of Ga_2O_3 by suboxide molecular-beam epitaxy. *Apl Materials*, *9*(3), 031101.

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11:30am **AC+MD-TuM-13 Microscopic-Scale Defect Analysis on Ga_2O_3 through Microscopy**, *M. Kim,* NIST-Gaithersburg, Republic of Korea; *A. Winchester, O. Maimon,* NIST-Gaithersburg; *S. Koo,* KwangWoon University, Korea; *Q. Li,* George Mason University; ***Sujitra Pookpanratana***, NIST-Gaithersburg

Crystalline defects of technologically mature materials have been identified and classified by the semiconductor industry [1,2], since it is economically beneficial to isolate failure mechanisms at the source rather than relying on backend testing. This has significantly improved device reliability. The various defects could be categorized into killer or non-killer defects, where killer defects can hinder the operation of high-performance devices by trapping charge carriers or causing increased leakage current. Although β-gallium oxide (β-Ga_2O_3) is expected to surpass silicon carbide (SiC), defects in Ga_2O_3 are prevalent and largely unclassified. Therefore, screening out defects that cause electrical device degradation must be solved for widespread adoption of β-Ga_2O_3.

In this work, photoemission electron microscopy (PEEM) is used to visualize micrometer-scale defects and determine their electronic impact. PEEM is based on the photoelectric effect and is a non-destructive analysis method where light is used to excite and eject electrons from the sample surface and these electrons are analyzed. We investigated the defects on commercially-available epitaxially-grown β-Ga_2O_3 on (010) β-Ga_2O_3 substrates. The epitaxy was formed by hydride vapor phase epitaxy (HVPE) with a target doping of $1x10^{18}$ cm^{-3} on the (010) semi-insulating β-Ga_2O_3 wafer. We identified elongated structures on the β-Ga_2O_3 epi-layer as shown in Figure 1a, and they appear in multiple instances of the sample surface and in a parallel configuration. These features resemble the "carrot" defect observed in SiC epitaxy [3]. From the imaging spectroscopy mode of the PEEM (Figure 1b), the base and tip of the carrot were found to have similar valence band maxima but dissimilar work functions. The spectra from the tip of the carrot resembles that of the surrounding β-Ga_2O_3 epi-layer. We are performing ongoing work to identify this feature as a microscopic defect. For understanding the electrical influence of these elongated features on HVPE epi-layer, we will perform tunneling atomic force microscopy (TUNA) to measure the electrical properties on and off the defect surface. Together, we will present a discussion on the nature of these distinct features and their implication on device performance.

11:45am **AC+MD-TuM-14 Characterization and Processing Improvements for Fabricating and Polishing β-Ga2O3 Substrates**, ***Robert Lavelle***, *D. Snyder, W. Everson, D. Erdely, L. Lyle, N. Alem, A. Balog,* Penn State University; *N. Mahadik, M. Liao,* Naval Research Laboratory

As progress continues to be made in fabricating and polishing uniform, high-quality β-Ga2O3 substrates, it is increasingly important to link commercial suppliers and research groups with expertise in crystal growth, substrate processing, epi growth/synthesis, characterization, and devices. This creates a vertically integrated feedback loop that drives answering fundamental research questions and increasing the manufacturability of the substrates. We will review our latest results in optimizing the chemi-mechanical polishing (CMP) methods and related processing steps for β-Ga2O3 substrates and materials characterization. This includes quantifying and minimizing subsurface damage related to processing, investigating the propagation of defects such as nanopipes, fabricating off-cut/off-axis substrates, and extending the fabrication/polishing methods to different alloy compositions.

Previous results showed that an excellent surface finish (Ra <2 Å over a >0.175 mm2 area) could be achieved for Czochralski (Cz) grown β-Ga2O3 substrates using a two-step CMP process with a nearly 10X reduction in polishing cycle time. After continuing to develop this process, we observed that a similar surface finish could be achieved by optimizing the pH of the colloidal silica slurry while realizing a further 3-4X reduction in cycle time. This establishes a path toward a milestone 1-day polishing process for β-Ga2O3 substrates. While the surface finish is similar, further reduction in the FWHM of the x-ray rocking curves (XRRCs) was also obtained by reducing the force and optimizing the other polishing parameters during the final CMP step. These processing changes suggest improvement in polishing related subsurface damage, which we assessed using high-resolution x-ray diffraction (HRXRD) by varying the x-ray penetration depth and advanced microscopy techniques.

Uniformity continues to be an important consideration as commercial 2"+ substrates become increasingly available. We continue to map and collect characterization data from across substrates grown by Cz and edge-defined film-fed growth (EFG) and will share our observations. This includes site-specific XRRC measurements as well as etch pit density (EPD) mapping and defect analysis for full substrates. In this discussion, we will also integrate feedback from epi growers for different types of substrates. Finally, we will discuss our methodology for processing off-cut/off-axis as well as alloyed substrates and latest characterization results.

Material and Device Processing and Fabrication Techniques
Room Davis Hall 101 - Session MD+AC+EP-TuA

Process/Devices II

Moderator: Yuhao Zhang, Virginia Tech

3:45pm **MD+AC+EP-TuA-9 Large Area Trench β-Ga_2O_3 Schottky Barrier Diode with Extreme-K Dielectric Resurf**, ***Saurav Roy,*** *A. Bhattacharyya,* University of California Santa Barbara*; J. Cooke,* University of Utah*; C. Peterson,* University of California Santa Barbara*; B. Rodriguez,* University of Utah*; S. Krishnamoorthy,* University of California Santa Barbara

We report the first combination of high-k dielectric RESURF with trench geometry to realize low reverse leakage large area (1mm^2 and 4mm^2) β-Ga_2O_3 Schottky Barrier Diodes with high current values (15A pulsed, 9A DC). 1.2 µm deep trenches are etched on HVPE-grown 11 µm epilayer with 8×10^{15} cm^{-3} apparent charge density concentration using dry etching and 300 nm $BaTiO_3$. (BTO)is then sputter deposited which is followed by annealing at 700°C to enhance the dielectric constant. The fins are then opened using dry etching. Pt/Au Schottky contacts are deposited using e-beam evaporation with planetary rotation for conformal deposition. To further improve the breakdown voltage field plates are used with Si_3N_4 as the field plate oxide. A planar SBD, a BTO field-plated SBD, and a trench SBD with high-k RESURF are fabricated for comparison. The on resistance ($R_{on,sp}$ normalized to the device footprint) of the planar and field plated SBDs are extracted to be 7.9 and 8.2 mΩ-cm^2, respectively, and an increased on resistance of 10.8 mΩ-cm^{-2} is measured for small area (200×200 μm^2) trench SBD with high-k RESURF, indicating dry etching induced damage. The breakdown voltage of the BTO field-plated SBD increases to 2.1 kV from 816 V (planar SBD) whereas the breakdown voltage increases to 2.8-3kV for the trench SBD with high-k RESURF. A very low leakage current density of 2×10^{-4} A/cm^2 is measured for the trench SBD at 2.8 kV. The 1 mm^2 trench SBD exhibits a current of 3.7A(Pulsed)/2.9A(DC) and the 4mm^2 trench SBD exhibitsa current of 15A(Pulsed)/9A(DC) at 5V. The breakdown (catastrophic) voltage of the 1mm^2 and 4mm^2 trench SBDs are measured to be 1.4 and 1.8kV. The leakage currents at breakdown are significantly lower compared to other high current SBDs reported in the literature despite the large area of the device, due to the much-reduced parallel field at the metal/semiconductor interface. Temperature dependence of on resistance shows lower temperature co-efficient (α = 0.87) which is lower than SiC SBDs. The large area high-k RESURF trench SBDs also has lowest $V_{on}I_{leakage}$ product for any β-Ga_2O_3 SBDs with more than 1kV breakdown voltage and 1A current, which is important to reduce both the on and off-state power dissipation. The 4mm^2 high-k RESURF trench SBD has the highest current (5A(DC)/9A(Pulsed)) at V_F = V_{on}+2V with breakdown voltage more than 1.3kV and exhibits lowest leakage current for similar rated device from literature.

This material is based upon work supported by the II-VI Block Gift Program and the Air Force Office of Scientific Research MURI award FA9550-21-0078.

4:00pm **MD+AC+EP-TuA-10 Fabrication and Characteristics of Ga_2O_3 MOSFET using p-NiO for Normally-off Operation**, ***Daehwan Chun,*** *Y. Jung, J. Park, J. Hong, N. Joo, T. Kim,* Hyundai Motor Company, Republic of Korea

In order to increase sales of electric vehicles, it is essential to have market competitiveness by reducing price and improving performance, as well as improving mileage. To increase the mileage of an electric vehicle, it is important to efficiently use the limited power of the battery. The inverter/converter/OBC plays a role in converting electrical energy into a form suitable for electrical components, and the power semiconductor performs switching and rectification operations in the components responsible for such power conversion. Therefore, the performance of power semiconductors is directly related to the mileage of electric vehicles.

Existing power semiconductors mainly used Silicon(Si) materials, but recently, Silicon Carbide(SiC) power semiconductors with improved performance have been mass-produced and started to be installed in vehicles. Gallium Oxide(Ga_2O_3), which has a wider energy bandgap(4.7~4.9eV) than SiC, has a high critical electric field, excellent electron transport ability, and high-quality large-area substrate growth, so it has the advantage of not only performance compared to existing GaN or SiC semiconductor but also easy manufacturing process. In particular, the unit price of Ga_2O_3 epitaxial wafer is expected to be reduced to 1/3 of that of SiC. Therefore, the manufacturing cost is also expected to be lower than that of SiC power semiconductors.

In this paper, we present the fabrication results of Ga_2O_3-based lateral MOSFETs for inverter/converter/OBC applications of electric vehicles. Normally-off operation was secured through the application of NiO, which does not require an ion implantation process, and a breakdown voltage of 600V was achieved. In addition, Al_2O_3 was used as a gate insulating film to suppress gate leakage current, and high-concentration ITO was applied to form an ohmic junction.

Applying NiO to form the depletion layer in the channel region when the MOSFET is off-state ensures normally-off operation of the Ga_2O_3 MOSFET. However, there is a limit to gate voltage application due to leakage current because of the existence of a pn heterojunction diode in the gate region. To solve this problem, an insulating film(Al_2O_3) was formed between NiO and the gate metal. The threshold voltage of the MOSFET with this structure formed a high value of 30V or more, so the threshold voltage was lowered by modifying the concentration of the Ga_2O_3 epitaxial layer. As a result, some drain-source leakage current occurred, but an IV characteristic graph that clearly distinguishes the On/Off state of the MOSFET was obtained.

4:15pm **MD+AC+EP-TuA-11 On the Mg-Diffused Current Blocking Layer for Ga_2O_3 Vertical Diffused Barrier Field-Effect-Transistor (VDBFET)**, ***Ke Zeng,*** *Z. Bian, S. Chowdhury,* Stanford University

To truly realize the potential of the Ga_2O_3 in a transistor, it is imperative to design a buried gate barrier junction to circumvent the pre-mature breakdown near the gate often seen in lateral structures. Owing to the high diffusivity of dopants and defects in Ga_2O_3, in contrast to that of, for example, SiC at a moderate temperature, we propose the use of diffusion doping as a rapid and non-invasive platform to explore the possibility of an effective current blocking layer (CBL) in vertical Ga_2O_3 transistors. In this work, we will discuss the development and characteristics of the Mg diffused CBL that was recently utilized to demonstrate an efficient Ga_2O_3 VDBFET with remarkable pinch-off characteristics.

The process (Fig. 1) starts with a commercially available Ga_2O_3 HVPE epitaxial wafer. The wafer was first coated with a highly Mg-doped spin-on-glass (SOG) layer which was subsequently cured and then patterned by HF to form the selective Mg dopant source. A thick PECVD layer was deposited onto the sample to isolate and stabilize the diffusion doping process. The Mg was then diffused into the wafer under a 950 °C furnace annealing for ~1 hr to form the CBL. The dopant oxide stack was stripped clean by an HF dip afterward. A Ni/Au anode was then deposited on top of the CBL region for the 2-terminal CV and IV studies shown in Fig. 2. Furthermore, for the 3-terminal VDBFET, a high dose titled Si triple ion implantation was done to form the source contact region inside the CBL area, followed by an activation annealing. The Ti/Au and Ni/Au composite source electrode was deposited on top of the source and CBL region respectively. A Ti/Au drain contact was then deposited on the back of the wafer. A 25nm ALD Al_2O_3 was used as the gate oxide, and a Ti/Ni/Au stack was deposited as the gate contact on top of the wafer.

From a simple CV analysis on the metal-isolation-semiconductor (MIS) structure, it's confirmed that the conductivity of the Ga_2O_3 epitaxial layer was successfully modulated by the Mg diffusion process for a depth of ~ 1.6 µm. The same MIS structure measured a reverse breakdown voltage of 466 V. However, when the surface is further doped with implanted Si^{++} layer, the formed NIN diode only blocks ~72V, the same as the final device blocking voltage. The VDBFET showed amazing transistor characteristics with decent saturation, on-current without any optimization, as well as a current on/off ratio > 10^9. Due to the compensation of electrons by Mg in the gate region, the transistor exhibited enhancement mode operation with a turn-on voltage of ~7V. The breakdown voltage, however, was only measured to be 72 V under a gate bias of 0 V.

4:30pm **MD+AC+EP-TuA-12 Electrical Properties of p-NiO/β-Ga_2O_3 Vertical PN Heterojunction Diode for Power Device Applications**, ***Youngkyun Jung,*** *D. Chun,* Hyundai Motor Company, Republic of Korea

In this paper, the p-type NiO/β-Ga_2O_3 vertical pn heterojunction diode for power device application was fabricated, and the electrical characteristics of the device was evaluated. The β- Ga_2O_3 has a wide energy bandgap of about 4.8eV, and that is expected to be a material for next-generation power semiconductors with high breakdown voltage and low power loss. Compared to SiC (Silicon carbide) and GaN (Gallium Nitride), which are used as common materials for power semiconductors, it has a breakdown field (8MV/cm) that is about 3 times higher, and Baliga's FOM (3,400), which represents the semiconductor figure of merit, it has a value 4 to 10 times higher than that of GaN and SIC materials. Recently, β-Ga_2O_3 has been fabricated in the form of an epitaxial layer on a wafer and applied to power devices such as MOSFETs, MESFETs, Schottky barrier diodes, and pn

junction diodes. The p-NiO has a wide band gap of 3.6 eV or more, p-type characteristics of NiO generally is induced by nickel vacancies or oxygen interstitials, that are defects provide the hole carriers. The carrier concentrations of p-NiO can be controlled in the range of 10^{16} to 10^{19} cm^{-3} with the amount of oxygen gas during the sputtering deposition process. The depletion region width of p-NiO/β-Ga_2O_3 can be changed according to the change in the carrier concentration of p-NiO. To fabricate the pn vertical heterojunction diode, p-NiO was deposited on the β-Ga_2O_3 epitaxial layer with a thickness of 250nm by using RF magnetron sputtering, and 100 nm of Ni metal for ohmic contact was deposited on the deposited p-NiO by using DC magnetron sputtering. The I-V characteristics of the fabricated pn heterojunction diode were measured by keithley 2410, and the C-V characteristics were measured by Keysight 4284A. As a result of measuring electrical characteristics, the pn heterojunction diode has a lower leakage current value than the previously reported Schottky Barrier Diode, and on/off ratio is about 10^9. When the carrier concentration of deposited p-NiO was $10^{19}cm^{-3}$, the turn-on voltage, current density, Ron value and breakdown voltage values of pn heterojunction diode were shown 2.2V, 242A/cm^2@4V, 17mΩ.cm^2@4V, and –465V respectively.

4:45pm **MD+AC+EP-TuA-13 Effects of Oxygen Reactive Ion Etching and Nitrogen Radical Irradiation on Electrical Properties of Ga_2O_3 Schottky Barrier Diodes**, ***Shota Sato***, *K. Eguchi,* Department of Physics and Electronics, Osaka Metropolitan University, Japan*; Z. Wang,* National Institute of Information and Communications Technology, Japan*; T. Kitada, M. Higashiwaki,* Department of Physics and Electronics, Osaka Metropolitan University, Japan

β-Ga_2O_3 has attracted great attention as a new wide bandgap semiconductor mainly for power devices. Oxygen reactive ion etching (O_2 RIE) is often used to remove a resist and/or an organic contamination in Ga_2O_3 device processing. However, this process usually causes damage to a Ga_2O_3 surface degrading device characteristics. On the other hand, we found that nitrogen (N) radical irradiation can significantly restore the Ga_2O_3 surface damage. In this study, we investigated effects of the O_2 RIE and N radical irradiation on electrical properties of Schottky barrier diodes (SBDs) fabricated on *β*-Ga_2O_3 (100) and (010) substrates.

Ga_2O_3 SBD structures were fabricated using unintentionally doped *β*-Ga_2O_3 (100) and (010) bulk substrates with an effective donor concentration of less than 2×10^{17} cm^{-3}. We evaluated electrical properties of the Ga_2O_3 SBDs fabricated on the substrates treated by four different processes: (a) no surface treatment, (b) O_2 RIE, (c) N radical irradiation, (d) O_2 RIE followed by N radical irradiation. The O_2 RIE was performed at an RF power of 50 W for 90 seconds. The N radical irradiation was conducted using an RF plasma cell in a molecular beam epitaxy growth chamber at a substrate temperature of 700°C and an RF power of 500 W for 2 hours.

We first studied current density–voltage (*J–V*) characteristics of the Ga_2O_3 (100) SBDs processed by the four different methods. In case of the devices with no treatment, a large variation of the turn-on *V* in a wide range of 0.5–1.1 V was observed. The O_2 RIE process further spread the variation to 0.2–1.0 V, indicating that the Ga_2O_3 (100) surface was more damaged. Furthermore, some devices showed kinks in their *J–V* curves. The curves with the kinks look like an overlap of *J–V* characteristics for a few area with different Schottky barrier heights under the anode electrode. In contrast, with and without the O_2 RIE, *J–V* characteristics of both SBDs treated by the N radical irradiation showed an almost constant turn-on *V* of 0.3 V and no kink. These results indicate that the N radical irradiation has effects to significantly restore the Ga_2O_3 surface damage and equalize the surface condition. Qualitatively the same effects of nitridation were confirmed for the Ga_2O_3 (010) SBDs.

In conclusion, we found that N radical irradiation is effective for restoring Ga_2O_3 surface damage, which leads to improvements in electrical properties of the Schottky interface.

This work was supported in part by the Development Program, “Next-Generation Energy-Saving Devices” of the Ministry of Internal Affairs and Communications, Japan (JPMI00316).

Material and Device Processing and Fabrication Techniques Room Bansal Atrium - Session MD-TuP

Material and Device Processing and Fabrication Techniques Poster Session II

MD-TuP-1 Growth of Room Temperature Polycrystalline β-Gallium Oxide Thin Film, ***Damanpreet Kaur***, *M. Kumar,* Indian Institute of Technology Ropar, India

Gallium oxide as an ultra-wide band gap semiconductor can exist in five different polymorphs – α, β, γ, κ, and ε – with different crystal structures and slightly different band gaps in the range of 4.6-5.3 eV.[1] The β-Ga_2O_3 is the most stable and most widely studied phase with intrinsic solar-blindness, band gap of 4.8 eV, high chemical and thermal stability, high breakdown voltage and high radiation hardness. Most of the existing literature have reported the fabrication of crystalline β-Ga_2O_3 at elevated temperatures (> 300°C) with no report on room temperature crystallization of gallium oxide.[2, 3] The material is either grown at a high temperature or it is annealed for achieving crystallization. The room temperature growth of gallium oxide is often reported to be amorphous in nature.

Herein, we report the formation of good quality polycrystalline β-Ga_2O_3 on *c*-plane sapphire at room temperature via RF Magnetron Sputtering. Grazing incidence X-ray Diffraction scans in the ϑ-2ϑ mode shows the peaks corresponding to the formation of polycrystalline peaks of β-Ga_2O_3. There is a shift in the peaks implying a strain in the films. Atomic Force Probe microscopy images reveal the formation of large grains which might be the cause of the strain in the films grown at room temperature. As a simple proof of concept, a photodetector with interdigitated Au electrodes was fabricated which showed a low dark current (~ 8 nA at +5 V) and a two order of magnitude (~ 0.46 μA at +5 V) enhancement upon 254 nm illumination.

References:

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MD-TuP-2 Performance and Traps of Ga_2O_3 Schottky Barrier Diodes with Mesa Structure, ***Min-Yeong Kim***, NIST-Gaithersburg, Republic of Korea; *O. Maimon,* NIST-Gaithersburg; *N. Hendricks, N. Moser,* Air Force Research Laboratory, USA; *S. Pookpanratana,* NIST-Gaithersburg; *S. Koo,* KwangWoon University, Korea; *Q. Li,* George Mason University

Among the ultrawide bandgap materials, Ga_2O_3 is expected to surpass the trade-off relationship between breakdown (BV) and on resistance ($R_{on,sp}$). However, the Ga_2O_3 vertical Schottky barrier diode (SBD) still cannot achieve the theoretical breakdown electric field. To improve electric field management, device designs incorporating field rings, junction termination extension, field plates, and mesa structure could be used to reduce the leakage current in the reverse bias state. The edge termination technique has been demonstrated to extend the breakdown voltage close to the ideal value that is determined by the material properties.[1] Fabricating mesa structures for edge termination can introduce defects and charge traps. Deep level traps can negatively affect the performance of devices by trapping charge carriers, resulting in reduced minority carrier lifetime and increased leakage current.

Here, we analyzed the characteristics of Ga_2O_3 SBDs with and without the mesa structure. The SBDs were fabricated on Si-doped β-Ga_2O_3 grown by halide vapor phase epitaxy (HVPE) on a Sn-doped ($6x10^{18}$ cm^{-3}) (001) β-Ga_2O_3 substrate. In the SBD with mesa structure, the circular mesa with a diameter of 162 μm and a depth of 500 nm was formed around anode electrodes. The Ti/Au metal stack on the polished back side of the substrate acted as a cathode while Ni/Au/Pt layers on the epitaxy acted as the anode electrode. After the fabrication process, current-voltage (I-V) measurements were performed as shown in Figure 1a. From the results, the $R_{on,sp}$ at 1 V are 6.9 Ω•cm^2 and 7.9 Ω•cm^2 in planar and mesa SBDs, respectively. In addition, the leakage current at -165 V is reduced by approximately 99.9% in the mesa structure. Figure 1 (b) shows the reverse bias characteristics of the SBDs, where the SBDs with mesa structure have approximately 2.75 times higher BV than SBDs without a mesa structure. Deep level defects were investigated by deep level transient spectroscopy (DLTS), and the SBDs with different structure have similar trap energy levels shown in Figure 2. In general, the trap density is larger in the SBD with mesa structures, however, the trap near the 3.0 eV is only detected for the SBD without the mesa structure and this defect is related to surface contamination. [2] Furthermore, we will extend the study by performing the cathodoluminescence (CL) spectroscopy to get radiative defect information of the SBDs which could be related to the DLTS results. We will discuss these results in light of the enhanced electrical performance of SBDs with mesa structures.

MD-TuP-4 Evolution of Lattice Distortions Throughout Various Stages of (010) β-Ga_2O_3 Substrate Preparation, ***Michael Liao***, National Research Council Postdoctoral at the U.S. Naval Research Laboratory; *N. Mahadik,* Naval Research Laboratory; *R. Lavelle, D. Snyder, W. Everson, D. Erdely, L. Lyle, N. Alem, A. Balog,* Penn State University; *T. Anderson,* Naval Research Laboratory

Meticulous preparation of substrates – in particular chemical mechanical polishing – is vital to many subsequent processes such as epitaxial growth, device fabrication and wafer bonding. After slicing substrates from boules, the rough substrates require lapping and polishing to achieve surfaces for epitaxial growth. However, lapping and aggressive polishing introduce sub-surface damage even if smooth surfaces are achieved.[1] Sub-surface damage manifests itself as lattice distortions such as tilt and strain, as well as generation of extended defects. The lattice distortions can be assessed using X-ray diffraction along different scanning axes. Previous work has been done to optimize polishing parameters to simultaneously achieve smooth (< 0.5 nm rms roughness) and subsurface-damage-free substrates.[2] Interestingly, it was found that the damage induced by wafer slicing was not only predominately lattice tilt, but the tilt was preferentially oriented along the [100] crystallographic axis. In this current work, we investigate the evolution of sub-surface damage of Czochralski-grown (010) β-Ga_2O_3 wafers that have undergone various preparation stages: wire sawn surfaces, lapping, and final polished surfaces. Multiple asymmetric reciprocal space maps (RSM) in the glancing incidence geometry were measured along different zone axes to deconvolve the contributions of lattice tilt and strain from sub-surface damage. For the wire sawn rough surface, the (420) RSM shows ~2.4× higher broadening along the ω-scanning axis, which is an indication that the nature of lattice distortion is predominately lattice tilt. Furthermore, this broadening was asymmetrical, which is an indication that the lattice tilt is anisotropic and could be related to the anisotropic elastic properties for various β-Ga_2O_3crystal planes. This was in contrast to the polished sample, where the distortion due to tilt was mostly removed, and there exists significantly reduced residual strain, indicated by small broadening in the ω:2θ scanning axis. These results are analyzed using the theoretical calculations of β-Ga_2O_3 elastic properties[3] to obtain insight on its unusual response to mechanical deformation during the wafer slicing and lapping process.

This research was performed while M.E.L. held an NRC Research Associateship award at the U.S. Naval Research Laboratory.

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MD-TuP-5 Investigation of In-Plane Anisotropy of In-situ Ga etching on (010) β-Ga_2O_3, ***Abishek Katta***, Arizona State University; *F. Alema, W. Brand, A. Osinsky,* Agnitron Technologies; *N. Kalarickal,* School of Electrical, Computer and Energy Engineering, Arizona State University

We report on 'in-situ' MOCVD Ga etching using the metal organic Ga precursor triethylgallium (TEGa) and the in-plane anisotropy of the etch characteristics. Etch rates exceeding 8μm/hr is demonstrated at high TEGa flow rates and a substrate temperature >900°C. Significant in-plane anisotropy in etching is observed on (010) β-Ga_2O_3 samples with trenches formed along [001] direction showing the smoothest sidewalls.

Many promising device structures used in Ga_2O_3, like trench SBDs, trench MOSFETs, FinFETs etc require fabrication of 3-D structures like fins and trenches. Several etch techniques have been reported, including ICP-RIE, wet etching and metal assisted chemical etching. However, most of these

techniques result in angled sidewalls and surface damage. Previously, exposure to metallic Ga was shown as a promising technique for etching Ga_2O_3, using the suboxide reaction 4Ga (s)+ Ga_2O_3 (s)—>3Ga_2O(g). In this work, we show that the suboxide reaction can also proceed by using TEGa as the Ga source with the Ga_2O_3 samples held at high temperature inside an MOCVD reactor.

The etching experiments were carried out in an Agnitron Agilis 100 MOCVD oxide reactor with a far injection showerhead. The variation in etch rate as a function of substrate temperature and TEGa flow rate was studied. Etch rate increases with substrate temperature till 900°C, above which no significant increase is observed. The etch rate also increases linearly with TEGa flow rate, eventually saturating at high flow rates. At T_{sub}=900°C and 1000°C, etch rates exceeding 8µm/hr is obtained, making it possible to fabricate deep trenches and high ASR 3-D structures. We also investigated in-plane anisotropy by using spoke wheel structures patterned on (010) β-Ga_2O_3 substrate (see Fig.2). The spoke wheel structure was etched at T_{sub}=800°C and TEGa flow rate of 12.1µmol/min to vertical etch depth of 2.5µm. In addition to vertical etching, lateral etching of the trenches was also observed, resulting in widening of the final trench widths. Using the final and initial trench widths, the ratio of lateral to a vertical etch rate was measured for various in-plane orientations on (010) β-Ga_2O_3. The lateral etch rate was found to be lowest for trenches oriented in the [001] direction (forms (100) sidewalls) and highest for fins oriented in the [102] directions (forms (-201) sidewalls). The trenches were also found to have vertical sidewalls which are ideal for fabricating sub-micron structures. The trench sidewalls along most orientations were found to be rough, however smooth sidewalls are obtained along [001] direction.

MD-TuP-6 Understanding Ohmic Contacts to N+ Doped (010) β-Ga_2O_3 by Both In-Situ MOCVD Doping and Silicon Ion Implantation, ***Kathleen Smith***, *K. Gann, C. Gorsak, N. Pieczulewski, H. Nair, M. Thompson, D. Jena, H. Xing,* Cornell University

Despite the promising properties of β-Ga_2O_3 for kV radio frequency (RF) applications, such as the large bandgap and critical electric field, decent carrier mobility, and availability of native substrates via many melt-growth techniques, Ga_2O_3 faces similar challenges to many wide bandgap semiconductors. Namely, the low electron affinity associated with the wide bandgap leads to few low work-function metals to form ohmic metal-semiconductor junctions. Instead, Ga_2O_3 relies on tunnel junctions between a metal and heavily doped regions for ohmic behavior. However, the reliable formation of such junctions is non-trivial.

In order to enable high speed device applications, the parasitic resistance from the contacts R_c should be much less than 1 Ω-mm. In this work, we demonstrate ohmic contacts well below this threshold both for ion-implanted and metal-organic chemical vapor deposition (MOCVD) grown heavily doped (N_d > 1E19 cm^{-3}) Ga_2O_3. We also show the resultant R_c can depend on subtle differences in Ga_2O_3 surface properties.

Ion-implanted samples were prepared by implanting Si into a 400 nm unintentionally doped epitaxial layer grown on an Fe-doped (010) β-Ga_2O_3 substrate to a box concentration of 5x10^{19} cm^{-3} over 100 nm, activated by a 20 minute anneal at 950 °C in dry UHP nitrogen. Transfer length method (TLM) patterns were then formed with Ti/Al/Ni (50/100/60 nm) ohmic contacts. The contacts were then alloyed by a series of rapid thermal anneals (RTA) in nitrogen ambient. The resulting TLM patterns had an R_c of 0.16±0.01 Ω-mm, and a sheet resistance R_{sh} of 237±2 Ω/□.

Heavily doped samples were also grown on Fe-doped (010) β-Ga_2O_3 via MOCVD, with in situ Si doping to a nominal concentration of 9x10^{19} cm^{-3} and a thickness of 150 nm. TLM patterns were made with Ti/Au (50/110 nm) contacts, and compared before and after post-contact deposition RTA. On some MOCVD samples, the unalloyed contacts show an extremely leaky Schottky behavior, with a measured R_c of 0.35±0.002 Ω-mm and an R_{sh} of 55±1 Ω/□ at a current bias of 50 mA. On others, the unalloyed contacts show a highly rectifying behavior. These also become ohmic post annealing; however, the resultant contacts were found to be extremely non-uniform spatially. We currently ascribe these abnormal contacts to the formation of a spatially non-uniform interfacial layer on the Ga2O3 surface. While these results demonstrate the attainability of low R_c, future efforts will be needed to carefully control the surface properties to reliably achieve low R_c and apply these contacts to the moderately doped channels desired for kV RF applications.

MD-TuP-7 Heteroepitaxial Growth of $ZnGa_2O_4$ by Post-Deposition Annealing of ZnO on Ga_2O_3 Substrate, ***Stefan Kosanovic***, *K. Sun,* University of Michigan, Ann Arbor*; U. Mishra,* University of California Santa Barbara*; E. Ahmadi,* University of Michigan, Ann Arbor

In recent years, β-Ga2O3 has attracted a great deal of interest for the next generation of power electronics due to its ultra-wide bandgap (~4.6 eV) and availability of native substrates. Spinel ZnGa2O4 is another ultra-wide bandgap semiconductor with similar bandgap (~4.6-5 eV) as Ga2O3. Moreover, in ternary spinel oxides, cations occupy octahedral and tetrahedral sites formed by oxygen atoms, leading to new possibilities for doping. Recent studies suggest that p-type doping in spinel ZnGa2O4 may be possible [1-3] Therefore, a Ga2O3-ZnGa2O4 heterostructure may enable design and fabrication of novel devices.

Several methods including sol-gel, RF magnetron sputtering, pulsed laser deposition, metalorganic chemical vapor deposition (MOCVD), and mist-CVD have been previously used for epitaxial growth of ZnGa2O4 on foreign substrates such as sapphire. Bulk ZnGa2O4 single crystal has also been fabricated using melt growth techniques [4]. Here we demonstrate a novel method for heteroepitaxial growth of high quality ZnGa2O3 on Ga2O3 substrate. In this method ZnO is first deposited by ALD on Ga¬2O3 followed by annealing at 900 C. TEM images revealed high structural quality of the film and a well-defined interface. SAED images showed that the ZnGa2O4 “semi-concurrently” matched to the Ga2O3 substrate, supporting high film quality. These results are demonstrated for the (-201), (001), and (010) Ga2O3 orientations.

[1] Z. Chi *et al*, Materials Today Physics, Vol. 20 (2021)

[2] Z. Chi *et al*, J. Phys. D: Appl. Phys. Vol. 56 (2023)

[3] E. Chikoidze *et al,* Cryst. Growth Des. Vol.20, 4 (2020)

[4] Z. Galazka *et al,* APL Mater. Vol 7, (2019

MD-TuP-8 Revitalizing Fractured β-Ga_2O_3 Nanomembranes: Nanogap Recovery for Enhanced Charge Transport Performance, *M. Hasan, J. Lai,* ***Jung-Hun Seo***, University at Buffalo

A free-standing β-Ga_2O_3, also called β-Ga_2O_3 nanomembrane, is an important next-generation wide bandgap semiconductor that can be used for myriad high-performance future flexible electronics. However, details of structure-property relationships of β-Ga_2O_3 NM under strain conditions have not yet been investigated. In this presentation, we systematically investigated the electrical properties of β-Ga_2O_3 NM under different uniaxial strain conditions using various surface analysis methods and revealed layer-delamination and fractures. The electrical characterization showed that the presence of nanometer-sized gaps between fractured pieces in β-Ga2O3 NM caused a severe property degradation due to higher resistance and uneven charge distribution in β-Ga_2O_3 NM which was also confirmed by the multiphysics simulation.

The degraded performance in β-Ga_2O_3 NM was substantially recovered by two different methods. (i) Saturated water vapor treatment: introducing excessive OH-bonds in fractured β-Ga_2O_3 NM via the water vapor treatment. The X-ray photoelectron spectroscopy study revealed that the formation of OH-bonds by the water vapor treatment chemically connected nano-gaps. (ii) Oxide passivation: deposition of a thin oxide layer such as Al_2O_3, HfO_2, and SiO_2 that is formed by an atomic layer deposition (ALD) system allows charges for hopping across fractured β-Ga_2O_3 pieces.

The treated β-Ga_2O_3 samples by the aforementioned method exhibited reliable and stable recovered electrical properties up to ~90 % of their initial values. Therefore, this result offers a viable route for utilizing β-Ga_2O_3 NMs as a next-generation material for a myriad of high-performance flexible electronics and optoelectronic applications.

MD-TuP-9 Impact of Magnetron Sputtered Ultra-Thin Layer of Fe-Doped β-Ga_2O_3 on Gallium Oxide Schottky Contacts, ***Adetayo Adedeji,*** Elizabeth City State University*; J. Merrett,* Air Force Research Laboratory, Aerospace Systems Directorate*; J. Lawson, C. Ebbing,* University of Dayton Research Institute

Adetayo Victor Adedeji[1], Jacob Lawson[2], Charles Ebbing[2], J. Neil Merrett[3]

[1] Elizabeth City State University, [2] University of Dayton Research Institute, [3] Air Force Research Laboratory

Ultra-thin layer (~ 4 nm) of Fe-doped ß-Ga_2O_3 was deposited by co-sputtering pure Ga_2O_3 and Fe targets on (010) n+ Sn-doped Ga_2O_3 epilayer grown by Halide Vapor Phase Epitaxy (HVPE) on Si-doped ß-Ga_2O_3 substrates. The HVPE epilayer was about 4.5 mm thick and 2E16 cm^{-3} doping concentration. The ultra-thin insulating layer was deposited at 600°C substrate temperature for 10 minutes in Ar/O_2 gas mixtures (5% O_2 by flow rate). 100W RF power was applied to the Ga_2O_3 target while the dopant target was sputtered with 9W DC power. Circular Ti contacts were deposited on a 5 mm x 5 mm sample by photolithography and magnetron sputtering. The sample was annealed in argon flow at 400°C after contact metallization. The I-V characteristics of the Schottky diodes showed that the reverse current of samples with ultra-thin Fe-doped ß-Ga_2O_3 is more that five orders of magnitude lower than samples without the ultra-thin layer while the forward current dropped by about one order of magnitude. Appreciable forward bias tunneling current was achieved with much lower reverse current compared with samples without insulating nanolayer. It has been demonstrated that this technique can be used to tune the barrier height of Schottky contacts to ß-Ga_2O_3. Such low leakage contacts can be useful in improving the performance of metal-semiconductor gates in MESFETs or in reducing the edge leakage of Schottky power diodes.

MD-TuP-10 An Investigation of (001) β-Ga_2O_3 Etching via Heated H_3PO_4, ***Steve Rebollo,*** *T. Itoh, S. Krishnamoorthy, J. Speck,* University of California, Santa Barbara

The fabrication of power devices that approach the β-Ga_2O_3 unipolar-FOM limit requires the use of field-management and RESURF techniques.[1] Utilizing dry etch processes for these techniques results in defect formation, which can impact the performance of devices.[2] Recently, Yuewei et al. used a wagon wheel pattern to explore the anisotropic etching behavior of (010) β-Ga_2O_3 in heated H_3PO_4. Compared to (010) β-Ga_2O_3, the (001) orientation is a better candidate for vertical power devices due to improved substrate scalability and slightly higher

PECVD was used to blanket deposit 533 nm of SiO_2 on Ga_2O_3. A wagon wheel pattern with 25 µm spoke widths was defined using photolithography. The spokes oriented along the [100] and [010] directions were carefully aligned to the edges of the substrates, which correspond to the (100) and (010) planes, respectively. Photoresist served as a mask to protect the SiO_2 during an HF etch. The SiO_2 etch rate was determined using Si substrates that were coloaded in the PECVD with the Ga_2O_3 substrate. Next, the sample was placed in a H_3PO_4/H_2O solution for 3.2 hours at a temperature of 140°C. The temperature was monitored and controlled using a temperature probe. The etch depth was determined via profilometry. Afterward, the sample was characterized via SEM.

Figure 1 shows an SEM image of the wagon wheel post-etch. The SiO_2 mask protecting the top of the spokes is still intact. Figure 2 shows a profile of the wagon wheel after etching. Assuming no significant SiO_2 etching[2], the (001) etch rate is 781 nm/hr. Figure 3 shows a 60°-tilted SEM image of a spoke oriented along the [-100] direction. An undercut of the SiO_2 mask can be observed. Since (010) is a mirror plane in β-Ga_2O_3, the spoke is symmetric about the (010) plane. Figure 4 shows the sidewall angles for the wagon wheel spokes. For spokes with an orientation in a positive k-direction, the right-hand sidewalls of the spokes were smooth and had low inclination angles and the left-hand sidewall exhibited roughness with a steeper inclination angle. The opposite was true for spokes oriented in the negative k-direction. This is another consequence of the mirror plane symmetry. The roughness could be the result of rough SiO_2 mask sidewalls. These findings can be useful for the development of dry-etch free process flows for high-performance devices.

[1] Li, Wenshen, et al. "1230 V β-Ga2O3 trench Schottky barrier diodes with an ultra-low leakage current of<1 µA/cm^2." *Applied Physics Letters* 113.20 (2018): 202101.

[2] Zhang, Yuewei, Akhil Mauze, and James S. Speck. "Anisotropic etching of β-Ga_2O_3 using hot phosphoric acid." *Applied Physics Letters* 115.1 (2019): 013501.

MD-TuP-11 An Organic, Direct Bonded Copper, Multi-Layered, Ultra-Low Inductance Package for High-Power UWBG MOSFETs, *J. Major, J. Calder, S. Zhao,* ***Faisal Khan,*** National Renewable Energy Laboratory

The most common metalized substrates used in high-power switching packages consist of a ceramic layer such as Aluminum Nitride (AlN) sandwiched between two copper layers. Ceramic substrates are used because it has the key characteristic of having high dielectric strength while being thermally conductive. A large drawback to ceramic substrates is that they do not allow for a multi-layered circuit design. By replacing the traditional ceramic substrate with organic direct bonded copper (ODBC) we can open a wide range of possibilities when it comes to power module layout such as multi-layered circuits and double-sided cooling. Both benefits are critical while packaging high-performance Gallium Oxide (Ga_2O_3) MOSFETs. Because of Ga_2O_3's relatively poor thermal conductivity, a double-sided cooled package becomes necessary. Therefore, the use of ODBC provides the flexibility to fabricate copper traces carrying much higher currents, and by creating a multi-layered package, we can drastically reduce the parasitic inductance inside the power module. Achieving lower parasitic inductance is critical for an ultra-fast Ga_2O_3 package to avoid excessive voltage overshoot and ringing. Using ODBC, we have designed novel packages capable of handling the challenges presented by fast Ga_2O_3 switching. Using multi-physics modeling software, we can validate our design before building the prototype. Due to the simple process parameters needed to work with ODBC, we can rapidly create prototypes without using external vendors. This flexibility allows us to quickly design, build, and validate highly complex switching power modules to accommodate next generation, Ga_2O_3 switching devices.

Epitaxial Growth
Room Davis Hall 101 - Session EG+BG+MD-WeM

Epitaxial III

Moderators: Hari Nair, Cornell University, **Uttam Singisetti**, University of Buffalo, SUNY

9:15am **EG+BG+MD-WeM-4 Growth of α-$(Al_xGa_{1-x})_2O_3$ by Suboxide Molecular-Beam Epitaxy**, ***Jacob Steele***, *K. Azizie, N. Pieczulewski, J. McCandless, D. Muller, H. Xing, D. Jena,* Cornell University*; T. Onuma,* Kogakuin University, Japan*; D. Schlom,* Cornell University (USA) and Leibniz-Institut für Kristallzüchtung (Germany)

Ga_2O_3 has attracted significant interest due to its ultra-wide bandgap, high electron mobility, and large breakdown field. These properties exceed the current benchmarks set by materials such as SiC and GaN, making Ga_2O_3 optimal for next-generation power devices. Still, it has been proposed that the properties of Ga_2O_3 can be extended further by alloying with Al to form $(Al_xGa_{1-x})_2O_3$ which can raise the bandgap to 8.6 eV. This goal presents a challenge for the most researched phase, β, as β-Ga_2O_3 thermodynamically prefers a monoclinic structure and α-Al_2O_3 is stable in the corundum structure. This structural mismatch limits the compositional range and the range of attainable bandgaps. In contrast, α-Ga_2O_3 occupies the corundum structure and has been shown to alloy over the full compositional range, enabling bandgaps from 5.3 - 8.6 eV. One method of growing α-$(Al_xGa_{1-x})_2O_3$ is molecular-beam epitaxy (MBE). MBE is a powerful and highly controllable growth technique for α-$(Al_xGa_{1-x})_2O_3$ thin films with drawbacks being slow growth rates of a few hundred nm/h and narrow adsorption-controlled growth windows. One method to improve the growth rate is the technique of suboxide MBE, which allows growth of β-Ga_2O_3 thin films at rates exceeding 1 µm/h with large adsorption-controlled growth regimes.

We show that suboxide MBE can be used for the epitaxial growth of high quality α-$(Al_xGa_{1-x})_2O_3$ thin films on A plane sapphire substrates over the full range of x at greater than 1 µm/h. For our study, gallium suboxide, Ga_2O, and elemental Al are the MBE sources. The oxidant is 80% distilled ozone which is held at constant pressure (5 x 10-6 Torr) while the Ga_2O and Al fluxes are varied to control composition. We measure the composition of our films with XRD and confirm that we cover the full range of $0 < x < 1$ with vacuum ultraviolet transmittance measurements showing that the bandgaps of our films shift from α-Ga_2O_3 to α-Al_2O_3. We show that the film composition can be controlled directly by the relative ratios of the Ga_2O and Al fluxes. Our films have high structural quality as revealed by the full width at half maximum (FWHM) of rocking curves of the α-$(Al_xGa_{1-x})_2O_3$ films ranging from 11 - 15 arcseconds; these FWHMs are identical to the underlying sapphire substrates. The surfaces of the films are also smooth with RMS roughnesses measured by atomic force microscopy ranging from 0.3 - 1.1 nm on α-$(Al_xGa_{1-x})_2O_3$ films with thicknesses in the 17.8 - 47.8 nm range. We also show our progress with growing α-$(Al_xGa_{1-x})_2O_3$ films over 100 nm thick and with doping using a SiO_2 source.

9:30am **EG+BG+MD-WeM-5 Structural, Electrical, and Thermal Characterization of CIS-MOCVD β-Ga_2O_3 Epitaxial Buffer Layers**, ***Hannah Masten***, Naval Research Laboratory*; G. Alvarez,* Cornell University*; C. Halverson,* Washington State University*; M. Liao, J. Lundh,* Naval Research Laboratory*; F. Alema, A. Osinsky,* Agnitron Technology*; A. Jacobs,* Naval Research Laboratory*; M. Weber,* Washington State University*; Z. Tian,* Cornell University*; K. Hobart, M. Tadjer,* Naval Research Laboratory

Epitaxial growth of β-Ga_2O_3 using metalorganic chemical vapor deposition (MOCVD) has seen great advancements demonstrating high-quality films with low point defect concentrations and high mobility with low doping concentrations [1]. Here, we investigate the impact of buffer layer thickness for these MOCVD epitaxial films on electrical characteristics, thermal conductivity, and defect concentrations.

MOCVD films were grown on Novel Crystal Technology's Fe-doped (010) β-Ga_2O_3 substrates using Agnitron Technology's Agilis close-injection showerhead MOCVD (CIS-MOCVD). The unintentionally doped (UID) buffer layer thickness was varied on the 3 samples: A-300, B-500, and C-1000 nm. The UID layers were followed by a 10 nm thick n^+ (~10^{19} cm^{-3}) Ga_2O_3 layer for improved channel conductivity. A 100 nm highly n^+ layer was selectively regrown following ref. [2]. Ohmic contacts were formed in the regrown areas with an annealed 20/200 nm Ti/Au metal stack (470 °C, 1 min., N_2). Mesa isolation was formed with an etch of ~170 nm. Transmission line measurements (TLM) showed sample C had the lowest specific contact resistance of 2.25 × 10^{-6}Ω·cm^2 and sample A had the highest of 1.99 × 10^{-4}Ω·cm^2. Room temperature Hall effect measurement showed similar mobility for B and C of 115-116 cm^2/V·s, while sample A showed a much lower mobility of 71 cm^2/V·s. Samples B and C, both showed high open-gated source-drain current (I_D) (>0.05 A/mm at V_{DS}= 5 V) and low isolation (mesa-mesa) current (I_{iso}) of < 0.1 µA/mm at V_{DS}= 10 V. Sample A (300 nm thick buffer layer), showed 10X lower open-gated I_D and a high I_{iso} of ~3 mA/mm at V_{DS}= 10 V. Higher I_{iso} for samples with thin buffer layers, such as sample A, have been frequently attributed to a peak in Si concentration at the epilayer/substrate interface observed in secondary-ion mass spectroscopy [1]. Here, we offer further insight on this effect via frequency-domain thermoreflectance (FDTR) and positron annihilation spectroscopy (PAS). Preliminary FDTR data showed decreasing thermal conductivity for thicker epilayers. PAS data fitted with a 3-layer model consistently showed higher density of Ga-related vacancies in the epilayers compared to each substrate. More detailed measurements, including XRD and device-level FDTR, will be performed. This preliminary data suggested that MOCVD Ga_2O_3 was affected by both unintentional impurities and point defects in addition to the known issue of interfacial Si accumulation. [1] A. Waseem, *et al., Physica Status Solidi (*A), p. 2200616, 2022. [2] Z. Xia, *et al.,IEEE EDL*, 39(4), 568–571, 2018.

9:45am **EG+BG+MD-WeM-6 Electrical and Optical Properties of Melt-Grown Mn Doped β-Ga_2O_3**, ***Benjamin Dutton***, *C. Remple, J. Jesenovec,* Washington State University*; J. Varley, L. Voss,* Lawrence Livermore National Laboratory*; M. McCluskey, J. McCloy,* Washington State University

Several acceptor dopants have been explored in β-Ga_2O_3 to produce semi-insulating substrates and epitaxial films. Fe and Mg make up the majority of research thus far, however, other transition metals provide potential alternatives for optimized performance. β-Ga_2O_3 bulk single crystals were grown by the Czochralski and vertical gradient freeze methods with a nominal dopant concentration of 0.25 at.% Mn. Ultraviolet-visible-near infrared spectroscopy and photoluminescence revealed polarization and orientation dependent optical absorptions and a unique orange luminescence. All samples were electrically insulating, indicative of acceptor doping on the order of 10^9 – 10^{11} ohm·cm at room temperature. Actual dopant concentrations of the intentionally doped transition metal and background impurities were determined via glow discharge mass spectrometry, indicating the macro-scale segregation behavior. Laser-ablation inductively-coupled plasma mass spectrometry along with photoluminescence mapping revealed micro-scale segregation of impurity ions. Density functional theory calculations were carried out to elucidate likely site-occupancy and the acceptor level of Mn in the band gap.

10:00am **EG+BG+MD-WeM-7 Mg and Zn Counter doping of Homoepitaxial β-Ga_2O_3 Grown by Molecular Beam Epitaxy**, ***Stephen Schaefer***, *K. Egbo, S. Harvey, A. Zakutayev, B. Tellekamp,* National Renewable Energy Laboratory

Gallium oxide has attracted attention as a candidate material for high-power diodes and transistors owing to its wide bandgap and high breakdown voltage. Homoepitaxial β-Ga_2O_3 has been successfully grown by plasma-assisted molecular beam epitaxy, however it is well-documented that unintentional Si donors at the epitaxial interface lead to the formation of an undesirable parasitic conducting channel. Mg and Zn are deep acceptor levels in β-Ga_2O_3 and Mg counterdoping by MBE has been shown to compensate unintentional donor impurities. However counterdoping with other elements such as Zn remains sparsely investigated.

We report on Mg and Zn counterdoping in homoepitaxial β-Ga_2O_3 grown by MBE on (010) Fe-doped (semi-insulating) and (001) Sn-doped (n-type) wafers. A valved cracker source is used for Mg while Zn is evaporated from a conventional effusion cell. Mg- and Zn-doped stacks are measured by secondary ion mass spectroscopy to calibrate the cell temperatures and valve positions to the dopant incorporation. A typical Ga_2O_3 growth temperature is 600 °C and growth rates are 0.47 – 0.70 Å/s. β-Ga_2O_3 samples composed of a ~2 nm Mg- or Zn-doped layer and a 300 nm unintentionally doped layer are grown with dopant fluxes ranging from 3.8×10^{-9} to 2.0×10^{-8} torr. Counterdoped samples grown on (001) Sn-doped and (010) Fe-doped wafers are processed into vertical and lateral Schottky devices, respectively. In both devices the Ohmic contact is formed by stable 5 nm Ti / 100 nm Au annealed under N_2 at 550 °C while the Schottky contact is formed by 30 nm Ni / 100 nm Au. The Schottky devices are characterized by capacitance-voltage (C-V) measurements at 20 kHz.

We find that the C-V characteristics of the vertical Schottky devices grown on (001) Sn-doped Ga_2O_3 show a reduction in residual capacitance and corresponding increase in depletion width at high reverse bias voltage for the Mg-counterdoped sample compared to an undoped control sample grown under identical conditions. Additionally, the I-V characteristic of the Mg doped device exhibits lower reverse leakage current. These findings are

mirrored in lateral Schottky devices grown on (010) Fe-doped Ga_2O_3 where counterdoping with 1.0×10^{-8} torr Zn flux results in approximately ~2× reduction of capacitance and effective carrier concentration while counterdoping with the same Mg flux results in ~5× reduction. The C-V results suggest that Mg and Zn effectively compensate unintentional donors in Ga_2O_3. Experiments including an annealing study of Mg and Zn diffusion in β-Ga_2O_3 are expected to yield insight to the controllability of counterdoping in Ga_2O_3.

10:15am **EG+BG+MD-WeM-8 Optimizing Si Implantation and Annealing in β-Ga_2O_3, *Katie Gann,*** *N. Pieczulewski,* Cornell University*; T. Asel,* Air Force Research Laboratory*; C. Gorsak,* Cornell University*; K. Heinselman,* national renewable Energy Laboratory*; K. Smith, J. McCandless,* Cornell University*; B. Noesges,* Air Force Research Lab*; G. Xing, D. Jena, H. Nair, D. Muller, M. Thompson,* Cornell University

Optimizing the thermal anneal of Si implanted β-Ga_2O_3 is critical for low resistance contacts and selective area doping in advanced device structures. We report the impact of annealing time, temperature, and ambient on the activation of ion-implanted Si in β-Ga_2O_3 at concentrations from 5×10^{18} to 1×10^{20} cm^{-3}, and in β-$(Al_xGa_{1-x})_2O_3$ (x≤15%) at 5×10^{19} cm^{-3}. Nearly full activation (>90%) and high mobilities (>70 cm^2/V-s) are achieved in β-Ga_2O_3 with contact resistances below 0.16 Ω-mm. In β-$(Al_xGa_{1-x})_2O_3$, initial results are promising with moderate activation (50%) and high mobility (60 cm^2/V-s).

UID β-Ga_2O_3 films were grown by plasma assisted MBE on Fe-doped (010) β-Ga_2O_3 substrates; comparable β-$(Al_xGa_{1-x})_2O_3$ films were grown by MOCVD. Si was implanted at multiple energies to yield 65 or 100 nm box profiles with concentrations of 5×10^{18}, 5×10^{19}, or 1×10^{20} cm^{-3}. To understand damage accumulation, low and high temperature implants were also studied. Anneals were performed in a UHV-compatible quartz furnace at 1 bar with well-controlled gas ambients.

To maintain β-Ga_2O_3 stability, P_{O2} must be greater than 10^{-9} bar (based on annealing in vacuum or forming gas). For 5×10^{19} cm^{-3} Si, full activation is achieved for $P_{O2}<10^{-4}$ bar while 5×10^{18} cm^{-3} tolerates ~10^{-2} bar. Water vapor is critical even at 1 ppm; at 25 ppm active carriers are reduced by 10x. Optimal results were obtained with H_2O below 10 ppb. Based on recovery with subsequent "dry" anneals, we propose an OH-mediated defect compensating Si dopants.

Lattice recovery (mobility) occurs for T > 900 °C, with carriers and mobility increasing with temperature to 1050 °C. However, SIMS shows substantial Si diffusion above 1000 °C with 950 °C the optimal anneal temperature. Activation at 950 °C is maximized between 5 and 20 minutes with shorter times exhibiting slightly lower mobilities while longer times result in carrier deactivation; this "over-annealing" behavior occurs at all temperatures and becomes more significant at high concentrations. Room temperature implants to 1×10^{20} cm^{-3} are shown to fully activate under these optimal conditions.

To understand lattice damage recovery, implants at varying temperatures were characterized by XRD, Rutherford Backscattering Channeling (RBS/C), and STEM. XRD showed no second phases under any conditions. RBS/C and STEM showed only partial amorphization with remnant aligned β-Ga_2O_3. We propose a model to explain the efficient activation based on 3D lattice recovery in the absence of full amorphization.

Electronic and Photonic Devices, Circuits and Applications
Room Davis Hall 101 - Session EP+ET+MD-WeM

Process/Devices III

Moderator: Marko Tadjer, Naval Research Laboratory

10:45am **EP+ET+MD-WeM-10 Recent Progress of Ga_2O_3 Power Technology: Large-Area Devices, Packaging, and Applications*, Yuhao Zhang,*** Virginia Tech **INVITED**

The Ga_2O_3 power device technology has witnessed fast advances towards power electronics applications. Recently, reports on large-area (ampere-class) Ga_2O_3 power devices have emerged globally, and their scope has gone well beyond the bare-die device demonstration into the device packaging, circuit testing, and ruggedness evaluation. These results have placed Ga_2O_3 in a unique position as the only ultra-wide bandgap semiconductor reaching these indispensable milestones for power device development. This talk will review the state of the art of the ampere-class Ga_2O_3 power devices (current up to >100 A and voltage up to >2000 V), covering the following topics:

1. Static electrical performance of Ga_2O_3 diodes and MOSFETs with ampere-class demonstrations (Fig. 1), with a summary of their key parameters including breakdown voltage, on-state current, and specific on-resistance (Fig. 2).
2. Dynamic performance of large-area Ga_2O_3 diodes and MOSFETs, including the reverse recovery, switching charge, as well as turn-ON and turn-OFF characteristics. A large-area Ga_2O_3 diode with NiO junction termination extension will be analyzed as a case study (Fig. 3).
3. Packaging and thermal management of Ga_2O_3 devices, highlighting the global efforts on junction-side packaging and cooling to overcome the low thermal conductivity of Ga_2O_3 (Fig. 4).
4. Circuit-level applications of Ga_2O_3 power devices, such as PFC circuits and double-pulse tests, as well as their circuit-level overcurrent/overvoltage ruggedness.

These results of large-area Ga_2O_3 devices allow for a direct comparison with commercial Si, SiC, and GaN devices. Accordingly, research opportunities and critical gaps for Ga_2O_3 power devices will also be discussed.

Reference:

[1] Y. Qin *et al.* , "Recent progress of Ga2O3 power technology: large-area devices, packaging and applications," *Jpn. J. Appl. Phys.*, vol. 62, no. SF, p. SF0801, Feb. 2023.

[2] Y. Qin *et al.*, "Thermal management and packaging of wide and ultra-wide bandgap power devices: a review and perspective," *J. Phys. Appl. Phys.*, vol. 56, no. 9, p. 093001, Feb. 2023.

[3] B. Wang *et al.*, "2.5 kV Vertical Ga2O3 Schottky Rectifier With Graded Junction Termination Extension," *IEEE Electron Device Lett.*, vol. 44, no. 2, pp. 221–224, Feb. 2023.

[4] B. Wang *et al.*, "Low Thermal Resistance (0.5 K/W) Ga_2O_3 Schottky Rectifiers With Double-Side Packaging," *IEEE Electron Device Lett.*, vol. 42, no. 8, pp. 1132–1135, Aug. 2021.

[5] M. Xiao *et al.*, "Packaged Ga2O3 Schottky Rectifiers With Over 60-A Surge Current Capability," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8565–8569, Aug. 2021.

11:15am **EP+ET+MD-WeM-12 Forward and Reverse Current Transport of (001) β-Ga_2O_3 Schottky Barrier Diodes and TiO_2/β-Ga_2O_3 Heterojunction Diodes with Various Schottky Metals, *Nolan Hendricks,*** AFRL, UCSB*; E. Farzana,* UCSB*; A. Islam, D. Dryden, J. Williams,* Air Force Research Lab*; J. Speck,* UCSB*; A. Green,* Air Force Research Lab

β-Ga_2O_3 (BGO) has great potential for power devices due to its predicted breakdown field of 8 MV/cm, ease of n-type doping, and availability of melt-grown native substrates. The TiO_2/BGO heterojunction diode (HJD) has been shown to reduce reverse current compared to Schottky barrier diodes (SBDs) due to the high permittivity of TiO_2 without significantly affecting forward conduction losses due to the band alignment. [1] We demonstrate SBDs and HJDs with Ni, Pt, Cr, and Ti contacts, analyzing the current transport mechanism and showing similar or lower conduction losses in the HJD for all metals and reduced leakage current at higher electric fields in reverse bias.

SBDs and HJDs were fabricated on 8.5 µm of Si-doped BGO grown by HVPE on a Sn-doped (001) BGO substrate. Fabrication began with a backside Ti/Au cathode. 6.5 nm of TiO_2 was deposited on the HJD sample by plasma-enhanced ALD. Circular anode contacts (D=150 µm) of Pt/Au, Ni/Au, Cr/Au, and Ti/Au (20/180 nm) were patterned by separate lithography steps.

Capacitance-voltage (C-V) behavior was measured at 1 MHz. N_D-N_A and Φ_B were extracted from $1/C^2$. Current-voltage-temperature (J-V-T) characteristics of each device were measured, and Richardson plots were created from fitting the exponential region of each curve. Φ_B and the Richardson constant (A*) were extracted from each plot. Φ_B extracted for HJD is lower than in the SBD for Ni and Pt, while it is slightly higher for Cr. Unlike the Ti SBD, the Ti HJD showed rectifying behavior and exponential J-V in forward bias. Φ_B from C-V was similar but lower than J-V-T. In the linear-scale forward J-V characteristics at 25 °C, the lower Φ_B leads to lower V_{on}. No meaningful change in differential $R_{on,sp}$ is seen.

The reverse J-V behavior of each device at 25 °C was measured up to breakdown. To compare devices with different doping, J_R is plotted against

the average electric field (E) at the BGO surface. In all cases, the HJDs saw higher E_{bk} than the corresponding SBDs. At lower field, the leakage current is higher in devices with lower Φ_B as expected from thermionic emission. However, at higher field, the leakage current is lower in all HJDs than the corresponding SBDs, indicating suppression of thermionic field emission current due to the wider energy barrier in the HJD. More detailed analysis indicating TFE as the primary leakage mechanism will be shown. Sharp increases in reverse current associated with defect-mediated soft breakdown are not observed for the HJDs. The reduced forward and reverse losses with higher V_{bk} of the TiO_2/BGO HJD demonstrate its potential to unlock the benefits of BGO in power diodes.

11:30am **EP+ET+MD-WeM-13 Vertical β-Ga_2O_3 Diodes with PtO_x/Interlayer Pt Schottky Contact and High Permittivity Dielectric Field Plate for Low Loss and High Breakdown Voltage**, ***Esmat Farzana***, *S. Roy, S. Krishnamoorthy, J. Speck,* University of California Santa Barbara

β-Ga_2O_3 is promising for high-power devices due to a bandgap of 4.8 eV, high breakdown field of 8 MV/cm, melt-grown substrates and shallow donors. However, the breakdown of β-Ga_2O_3 Schottky barrier diode (SBD) is often dictated by tunneling leakage through metal Schottky contacts with a limited Schottky barrier height (SBH) of 1.5 eV. Although oxidized noble metals (e.g, PtO_x) with SBH>2 eV can reduce tunneling leakage and improve breakdown voltage, the trade-off comes with increased on-state loss. Here, we report an alternative scheme of composite Schottky contact, PtO_x/Interlayer Pt, as a solution of reducing leakage but minimizing turn-on loss compared to PtO_x. As shown with vertical GaN SBDs,[1] the sputtered PtO_x with an interlayer e-beam deposited Pt, can reduce leakage, increase breakdown voltage, while enabling low turn-on voltage. Moreover, for edge leakage management, we integrated high permittivity ZrO_2 field-plate in these SBDs.

The SBDs were fabricated on halide vapor phase epitaxy (HVPE) (001) β-Ga_2O_3 of 10 µm epitaxy (doping ~1×10^{16} cm^{-3}). Three different Schottky contacts were fabricated, Pt, PtO_x (24 nm)/Interlayer Pt (1.5 nm), and PtO_x (24 nm). The PtO_x/Interlayer Pt SBDs were also investigated with a field-plate dielectric of 100 nm ZrO_2 (dielectric constant~26) on top of a 11 nm Al_2O_3 formed by atomic layer deposition (ALD) to protect the surface from sputtering-induced damage.

In bare SBDs, the forward current density-voltage (J-V) provided near unity ideality factor and SBHs of Pt (1.1 eV), PtO_x/Interlayer Pt (1.49 eV) and PtO_x (1.90 eV). The $1/C^2$-V provided similar trend of SBH with Pt (1.48 eV), PtO_x/Interlayer Pt (1.92 eV) and PtO_x (2.28 eV). Thus, the interlayer Pt allows tuning of SBH to lower values than PtO_x, leading to lower turn-on loss. All SBDs showed punchthrough breakdown where the fully depleted condition is reached at -910 V (estimated). The bare PtO_x/Interlayer Pt SBDs showed lower leakage and higher breakdown voltage (V_{br}) of 1.76 kV compared to Pt with 1.32 kV. The ZrO_2 field-plate further increased V_{br} to 2.34 kV. With a minimum on-resistance of 8 mΩ-cm^2, the Baliga's figure-of-merit (BFOM) of the field-plate SBD was obtained as 0.684 GW/cm^2. SILVACO simulation showed a parallel plane peak field of 3.25 MV/cm at anode center, peak field of 8 MV/cm at edge in β-Ga_2O_3, and 8.86 MV/cm in Al_2O_3. The barrier height engineering and field management involving processing techniques with reduced or minimal material damage presented here is promising for realizing robust high performance β-Ga_2O_3 vertical power devices.

[1] Z. Shi et al., Semi. Sci. Tech. 37, 065010 (2022).

11:45am **EP+ET+MD-WeM-14 Ni/TiO_2/β-Ga_2O_3 Heterojunction Diodes with NiO Guard Ring Simultaneously Increasing Breakdown Voltage and Reducing Turn-on Voltage**, *J. Williams, N. Hendricks,* Air Force Research Lab*;* ***Weisong Wang,*** Wright State University*; A. Adams,* Apex Micro Devices*; J. Piel, D. Dryden, K. Liddy,* Air Force Research Lab*; N. Sepelak,* KBR Inc.*; B. Morell,* Cornell University*; A. Miesle,* University of Dayton*; A. Islam, A. Green,* Air Force Research Lab

β-Ga_2O_3 is an ultra-wide bandgap semiconductor (~4.8 eV) with numerous merits that potentially surpass the material limits other semiconductors for power electronic applications, namely a high predicted critical field strength of 8 MV/cm. Vertical Schottky barrier diodes (SBD) are a fundamental application for β-Ga_2O_3 to demonstrate power handling capabilities. However, breakdown behavior is limited by electric field crowding at the contact edge and high tunneling current under large reverse bias. We are reporting a novel integration of vertical heterojunction diode based on Ni/TiO_2/β-Ga_2O_3 with p-type NiO as the guard ring (GR). The heterojunction improves off-state losses and breakdown voltage (V_{bk}) without adding significant on-state losses. Leakage current is reduced by the additional barrier width, but the negative conduction-band offset between TiO_2 and β-Ga_2O_3 maintains low V_{on}. P-type NiO guard ring is to surround heterojunction to screen the high electric field generated at this region.

The devices were fabricated on an 8.5 µm Si-doped β-Ga_2O_3 drift region grown by HVPE on a heavily Sn doped (001) substrate. A back-side Ohmic contact was formed by evaporated Ti/Au. The NiO GR was created by sputtering and lift-off. A thin TiO_2 layer (42 Å) by ALD was shaped to overlap the anode. The Ni/Au anode was deposited before mesa was etched to provide edge termination to the SBD and HJD. The devices have circular contacts (D=100 µm) with an additional 5 µm GR. SBDs were co-fabricated on the same substrate as references. HJD showed a lower V_{on} (0.8 V) than the SBD (1.1 V) from linear extrapolation of the J-V curve. Temperature dependent I-V behavior was measured from 25 ºC to 200 ºC. Both device types show excellent fits to the thermionic emission model, and barrier heights of 0.6 eV and 1.2 eV were fit for the HJD and SBD respectively. The HJD had higher V_{bk} of 1190 V compared to the SBD (685 V), and the GR HJD saw even further improvement with V_{bk} of 1777 V (826 V for GR SBD). The BFOM ($V_{bk}^2/R_{on,sp}$) of 518 MW/$cm^2$for the GR HJD is competitive with other literature results.

This work demonstrates an average breakdown field beyond the material limits of SiC and GaN in a device that has even lower conduction losses than the co-fabricated SBD. Lowering V_{on} while raising V_{bk} simultaneously improves both on- and off-state parameters that are typically in competition with each other. With further optimized field management, the Ni/TiO_2/β-Ga_2O_3-HJD presents a path to realistically utilizing the high critical field of Ga_2O_3 without large forward conduction losses from a high-barrier junction.

12:00pm **EP+ET+MD-WeM-15 Fabrication of Self Aligned β-Ga_2O_3 Junction Barrier Schottky Diodes with NiO Field Termination**, ***Joseph Spencer,*** Naval Research Laboratory*; B. Wang, M. Xiao,* Virginia Tech*; A. Jacobs, T. Anderson, K. Hobart,* Naval Research Laboratory*; Y. Zhang,* Virginia Tech*; M. Tadjer,* Naval Research Laboratory

While the ultra-wide bandgap (4.8 eV) and the high critical field (6-8 MV/cm) of Ga_2O_3 is promising, the lack of shallow acceptors and the self-trapping of holes prevents this material from being doped p-type. The lack of complementary conductivity limits the practical device and termination structures for Ga_2O_3. Without the availability of p-type Ga_2O_3, Ga_2O_3 power devices must rely on a heterojunction for forming critically-important pn junctions. The naturally p-type nickel oxide (NiO, 3.6-4.5 eV [1]) forms a heterojunction with Ga_2O_3 and has been used to demonstrate Ga_2O_3 JBS diodes [2, 3].

In this work we have developed a self-aligned JBS diode fabrication process at 1 µm resolution that is capable of withstanding high-temperature thermal and chemical treatments such as annealing and relevant plasma/acid etches for Ga_2O_3 (e.g., BCl_3, HCl, H_3PO_4). This novel dry lift-off process incorporates a XeF_2 etch for undercut and lift-off steps producing a self-aligned process enabling fine device features without misalignment. A tri-layer mask consisting of, in order of deposition, amorphous Silicon (a-Si), SiO_2, and Ni, allow for the dry etching of the Ga_2O_3 epilayer prior to NiO self-aligned deposition. The Ni, SiO_2, and a-Si layers were patterned using Transene Ni-etchant, CF_4-plasma, and a SF_6-plasma dry etching, respectively. Subsequently, a ~250 nm deep trench in the Ga_2O_3 epilayer was etched via BCl_3 plasma, and a post-dry etch clean in warm (80 °C) H_3PO_4 was performed for 10 minutes, wherein the Ni hard mask was also removed. The a-Si mask layer was undercut using a 1" burst of dilute XeF_2 in a Xactix XeF_2 etcher. P-type NiO with 10% O_2 was sputtered (200 W, 12.5 mTorr) in the trench regions, followed by a dry lift-off of the remaining mask (a-Si/SiO_2) in XeF_2 gas by selective undercutting of the a-Si layer. At the conclusion of this self-aligned process, a tri-layer NiO junction termination extension (JTE) region was deposited around the anode perimeter in order to facilitate electric field spreading and improve V_{BR} [4]. Ni/Au anode was deposited atop the JBS region and the inner portions of the NiO JTE to conclude device fabrication (Figs. 1-4). Current-voltage characteristics in forward and reverse bias are shown in Figs. 5-6, respectively. This novel self-aligned process as shown by the fabrication of Ga_2O_3 NiOJBS diode serves to advance Ga_2O_3 heterojunction device technology and fabrication capabilities.

12:15pm **EP+ET+MD-WeM-16 Ni/$BaTiO_3$/β-Ga2O3 Solar-Blind UV Photodetectors with Deep Etch Edge Termination**, ***Nathan Wriedt***, *S. Rajan,* Ohio State University

We report on the design and demonstration Ni/$BaTiO_3$/β-Ga_2O_3 photodetectors, where high-permittivity $BaTiO_3$ is introduced to enable high fields approaching the material (avalanche breakdown) limit. β-Ga_2O_3

has a bandgap of 4.8eV and a corresponding photon absorption edge at 270-280nm, making it a prime candidate for utilization in solar blind UV photodetectors applications. Furthermore, the excellent material quality and low doping densities achievable through epitaxy on bulk-grown substrates can enable extremely low dark currents. Schottky diodes suffer breakdown well before the 8 MV/cm material limit. However, inserting the extreme-k $BaTiO_3$ dielectric between the metal and β-Ga_2O_3 prevents tunneling breakdown of the metal-semiconductor interface, and has been shown to support extremely high breakdown fields in β-Ga_2O_3 [1].When high electric fields occur in the β-Ga_2O_3 the electric field in the $BaTiO_3$ is low due to the relative permittivity, thus maintaining a tunneling barrier. Additionally, the valence band offset between the $BaTiO_3$ and Ga_2O_3 presents no barrier to transport of holes. Device were fabricated using (001)-oriented HVPE-grown Ga_2O_3 films (10-µm, N_d=1x10^{16} cm^{-3}) on Sn-doped Ga_2O_3 bulk substrates. The device structure investigated consisted of 1000 µm diameter circular mesas where the epitaxial layer was etched using a BCl_3/Cl_2-based ICP-RIE process to produce 0, 3, and 6-um pillars that have been shown to be effective in achieving high junction termination efficiency [2]. 10 nm $BaTiO_3$ was then deposited conformally by RF sputtering onto the etched surface. Device fabrication was completed by e-beam evaporation of Ti/Au backside ohmic contact and Ni top contacts. Extremely low dark currents (~0.25nA/cm^2) were measured under reverse bias up to 200 V. The devices showed an excellent UV/visible rejection ratio [R(244)/R(400)=3.65 *10^7]. We estimated the peak responsivity to be 970 mA/W at 244 nm at a reverse bias of -20 V. In conclusion, the work here shows the promise of Ni/$BaTiO_3$/β-Ga_2O_3 for realizing photodetectors with excellent operating characteristics. This work lays the foundation for future studies where the high breakdown strength enabled by $BaTiO_3$ could enable the design of solar-blind photodetectors with avalanche gain. We acknowledge funding from Department of Energy / National Nuclear Security Administration under Award Number(s) DE-NA0003921, and AFOSR GAME MURI (Award No. FA9550-18-1-0479, project manager Dr. Ali Sayir).[1] Xia et al, Appl. Phys. Lett. 115, 252104 (2019)[2]Dhara et al, Appl. Phys. Lett. 121, 203501 (2022)

12:30pm **EP+ET+MD-WeM-17 Best Paper Awards, e-Surveys, and Closing Remarks**,

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