Electronic and Photonic Devices, Circuits and Applications
Room Davis Hall 101 - Session EP+HM+MD-MoA

Processes/Devices I
Moderator: Yuhao Zhang, Virginia Tech

1:45pm **EP+HM+MD-MoA-1 Gallium Oxide – Heterogenous Integration with Diamond for Advanced Device Structures**, *H. Kim, A. Bhat, A. Nandi, V. Charan, I. Sanyal, A. Mishra, Z. Abdallah, M. Smith, J. Pomeroy, D. Cherns,* ***Martin Kuball,*** University of Bristol, UK **INVITED**

Potentials for heterogenous integration of Ga_2O_3 with high thermal conductivity materials such as diamond for enabling energy-efficient kV-class power devices are being discussed. The integration alleviates Ga_2O_3 material drawbacks such as its low thermal conductivity and inefficient hole conductivity. The benefits of heterogeneous integration are for example demonstrated through electrical and thermal simulations of a Ga_2O_3-Al_2O_3-diamond superjunction based Schottky barrier diode. The simulation studies show that the novel device has potential to break the R_{ON}-breakdown voltage limit of Ga_2O_3, while showing relatively low rise in temperature compared to conventional devices. As step into their realization, experimental Al_2O_3 assessment namely ledge features in the capacitance-voltage (CV) profiles of Ga_2O_3 metal-oxide-semiconductor (MOS) capacitors were investigated using UV-assisted CV measurements; an interface trapping model is presented whereby the capacitance ledge is associated with carrier trapping in deep-level states at the Al_2O_3/Ga_2O_3 interface. Trench-Schottky Barrier diodes with breakdown voltage in excess of 1.5kV were demonstrated. First steps for the materials integration of Ga_2O_3 with diamond towards a superjunction based trench-Schottky barrier diode, including epitaxial growth of Ga_2O_3 on single crystal diamond substrates are being reported.

2:15pm **EP+HM+MD-MoA-3 Highly Scaled β-Ga2O3 MOSFET with 5.4 MV/cm Average Breakdown Field and Near 50 GHz fMAX**, ***Chinmoy Nath Saha,*** *A. vaidya,* SUNY at Buffalo*; A. Bhuiyan, L. Meng,* Ohio State University*; S. Sharma,* SUNY at Buffalo*; H. Zhao,* Ohio State University*; U. Singisetti,* SUNY at Buffalo

This letter reports the high performance β-Ga2O3 thin channel MOSFET with T gate and degenerately doped source/drain contacts regrown by Metal Organic Chemical Vapour Deposition (MOCVD). Device epitaxial layer was grown by Ozone MBE. Highly scaled T-gate (LG=160-200 nm) was fabricated to achieve enhanced RF performance and passivated with 200 nm Silicon Nitride (Si3N4). Peak drain current (ID,MAX) of 285 mA/mm and peak trans-conductance (gm) of 52 mS/mm were measured at 10 V drain bias with 23.5 Ω mm on resistance (Ron). Metal/n+ contact resistance of 0.078 Ω mm was extracted from Transfer Length Measurements (TLM). Channel sheet resistance was measured to be 14.2 Kiloohm/square from cross bar structure. Based on TLM and cross bar measurements, we determined that on resistance (Ron) is possibly dominated by interface resistance between channel and regrown layer. Different growth methods originating from MBE channel layer and MOCVD regrown n++ layer can cause this high interface resistance. A gate-to-drain breakdown voltage(V_{DG}) of 192 V is measured for L_{GD}= 355 nm resulting in average breakdown field (E_{AVG}) of 5.4 MV/cm. This $E_{AVG}$is the highest reported among all sub-micron gate length lateral FETs. And highest overall without using any intentional field plate techniques. Current gain cut off frequency (f_T) of 11 GHz and record power gain cut off frequency (f_{MAX}) of approximately 48 GHz were extracted from small signal measurements. f_T is possibly limited by DC-RF dispersion due to interface traps which need further investigation. We observed moderate DC-RF dispersion at 200 ns pulse width (for both output and transfer curve) which can corroborate our theory. We recorded f_T.V_{BR} product of 2.112 THz.V for 192 V breakdown voltage which is similar to GaN HEMT devices. Our device surpasses the switching figure of merit of Silicon because of low on resistance and high breakdown voltage, and competitive with mature wide-band gap devices. Proper surface cleaning between channel and regrowth layer and sub-100 nm T gate device structure can pave the way for better RF performance.

2:30pm **EP+HM+MD-MoA-4 Demonstration of a β-Ga_2O_3 Lateral Diode Full-Wave Rectifier Monolithic Integrated Circuit**, ***Jeremiah Williams,*** *J. Piel, A. Islam, N. Hendricks, D. Dryden, N. Moser,* Air Force Research Laboratory, Sensors Directorate*; W. Wang,* Wright State University*; K. Liddy, M. Ngo,* Air Force Research Laboratory, Sensors Directorate*; N. Sepelak,* KBR Inc.*; A. Green,* Air Force Research Laboratory, Sensors Directorate

Beta Gallium Oxide (Ga_2O_3) is well positioned excel in high power density applications due to its wide band gap, critical field strength, multiple shallow donor species, and melt grown native substrates. Monolithic integrated circuits (ICs) can advance Ga_2O_3 by reducing the size, weight, and connectivity parasitics of components. Lateral topologies with thin epitaxy on insulating substrates enable simple fabrication and integration of RF components. This work utilizes this system to demonstrate a fundamental circuit, the diode full-wave rectifier, with an accompanying design study of the interdigitated lateral diode topology.

The devices (Fig. 1) are fabricated from a 65 nm Si-doped Ga_2O_3 epitaxial layer grown by MBE on a Fe-doped Ga_2O_3 substrate. Epitaxy carrier concentration is measured to be 2×10^{18} cm^{-3} from C-V test structures (Fig. 2). The cathode is a Ti/Al/Ni/Au Ohmic contact annealed at 470 °C. The devices are isolated with a BCl_3 ICP mesa etch. A field-plate and surface passivation oxide of 80 nm thick Al_2O_3 is deposited by ALD. The anode is a Ni/Au Schottky contact. A full-wave rectifier and 16 diode variations are evaluated. The diodes have square and rounded contacts; anode finger counts of 1, 2, 4, and 8; and anode-cathode lengths ($L_{A\text{-}C}$) of 5, 7, and 12 µm. Anode length is 4 µm and width is 48 µm. The diodes in the rectifier have round contacts, 4 anode fingers, and 12 µm $L_{A\text{-}C}$ (Fig. 3). The rectifier is measured on-chip with micro probes. An AC signal is generated with a high-voltage amplifier and measured on an oscilloscope. The output of the rectifier to a 47 kΩ load is measured differentially, using a voltage divider to protect the oscilloscope from voltage spikes (Fig. 4).

The rectifier successfully demonstrates full-wave rectification of sine waves up to 144 V_{rms} (205 V peak) and 400 Hz (Fig. 5). The rectifier demonstrates 83 % efficiency and 0.78 W peak power. To the authors' knowledge, this is the first demonstration of a diode full-waver rectifier IC in Ga_2O_3. From the lateral diode design study, rounded contacts improve the average breakdown voltage (V_{bk}) by 20% (+41 V) without effecting specific on-resistance ($R\text{-}_{on,sp}$) (Fig. 6). The number of anode fingers does not statistically affect V_{bk}, and improves average $R\text{-}_{on,sp}$ by 18% (-0.45 mΩ-cm^2) at eight (Fig. 7). Scaling $L_{A\text{-}C}$ to 5, 7, and 12 µm also scales average $R_{on,sp}$ to 2.0, 2.9, and 8.6 mΩ-cm^2. Average V_{bk} scales as well, but with no change between 5 and 7 µm $L_{A\text{-}C}$ (248, 242, and 341 V) (Fig. 8). The J-V characteristics of a single diode (round contacts, eight fingers, 5 µm $L_{A\text{-}C}$) are included in Fig. 9.

2:45pm **EP+HM+MD-MoA-5 Improved Breakdown Strength of Lateral β-Ga_2O_3 MOSFETs Using Aerosol-Spray-Printed hBN-BCB Composite Encapsulation**, ***Daniel Dryden,*** Air Force Research Laboratory, Sensors Directorate*; L. Davidson,* KBR, Inc.*; K. Liddy, J. Williams, T. Pandhi, A. Islam, N. Hendricks, J. Piel,* Air Force Research Laboratory, Sensors Directorate*; N. Sepelak,* KBR, Inc.*; D. Walker, Jr., K. Leedy,* Air Force Research Laboratory, Sensors Directorate*; T. Asel, S. Mou,* Air Force Research Laboratory, Materials and Manufacturing Directorate, USA*; F. Ouchen,* KBR, Inc.*; E. Heckman, A. Green,* Air Force Research Laboratory, Sensors Directorate

Beta gallium oxide (β-Ga_2O_3) has shown promise for high-voltage power devices and power switching due to its large critical field strength E_c estimated at 8 MV/cm [1]. Dielectric passivation and testing under Fluorinert immersion [2] are used to increase breakdown voltage V_{bk} and avoid air breakdown, respectively, with the highest V_{bk} lateral Ga_2O_3 devices using polymer passivation [3]. The polymer benzocyclobutene (BCB) exhibits high dielectric strength, low parasitics, and good manufacturability [4,5]. It may be loaded with hexagonal boron nitride (hBN), improving thermal conductivity, dielectric response, and mechanical durability [6]. Coatings can be applied via aerosol jet printing, allowing multiple experimental conditions across devices on a single sample. Here, lateral β-Ga_2O_3 MOSFETs encapsulated with hBN-loaded BCB (hBN-BCB) which exhibit significantly enhanced V_{bk} compared to devices encapsulated with BCB alone or without encapsulation.

Si-doped β-Ga_2O_3 was grown epitaxially on a semi-insulating, Fe-doped (010) Ga_2O_3 substrate via molecular beam epitaxy to a nominal thickness of 65 nm and a doping of $2.8\text{+-}0.2\text{x}10^{17}$ cm^{-3}. Ti/Al/Ni/Au ohmic contacts were deposited and annealed at 470 °C for 60 s in N_2. Ni/Au gates were deposited on a gate oxide of 20 nm Al_2O_3, followed by a passivation oxide of 85 nm Al_2O_3. Thick Au contacts were formed using evaporation and electroplating. Devices with BCB or hBN-BCB were encapsulated using an

Optomec AJ200 aerosol jet printer. Inks consisted of Cyclotene 4022-35, cyclohexanone and terpineol, with or without hBN.

V_{bk} was tested under air or Fluorinert (Figure 2). Devices tested under Fluorinert, BCB, and BCB plus Fluorinert showed a 1.7x improvement in V_{bk} over air. Devices with hBN-BCB showed an improvement of 3.7x over air and 1.35x over BCB alone. The hBN-BCB-coated devices (N=6) show significant improvement in V_{bk} over the devices coated BCB alone (N=3) with p<0.011 (single-tail heteroscedastic T-Test).

Device performance of the highest-V_{bk} device are shown in Figure 3. The device, before encapsulation, had R_{on} of 683 Ω·mm, I_{max} of 3.42 mA/mm, $G_{m,peak}$ of 1.14 mS/mm, V_{th} of -3.8 V, V_{off} of -6.5 V, and V_{bk} of 951 V ($E_{crit,avg}$ 1.23 MV/cm). Device performance was unaffected by hBN-BCB encapsulation (Fig. 3b) excepting a change in V_{off} to -8 V. No significant gate leakage was observed during device operation or breakdown. Breakdown likely occurred due to peak fields exceeding the E_{crit} of one or more materials at the drain-side edge of the gate. These results provide a significant improvement over existing encapsulation approaches in β-Ga_2O_3 lateral MOSFETs.

3:00pm **EP+HM+MD-MoA-6 Wafer-Scale β-Ga_2O_3 Field Effect Transistors with MOCVD-Grown Channel Layers**, ***Carl Peterson***, University of California Santa Barbara*; F. Alema,* Agnitron Technology Incorporated*; Z. Ling, A. Bhattacharyya,* University of California Santa Barbara*; S. Roy,* University of California at Santa Barbara*; A. Osinsky,* Agnitron Technology Incorporated*; S. Krishnamoorthy,* University of California Santa Barbara

We report on the growth, fabrication, and wafer-scale characterization of lateral high-voltage MOSFETs with ~120-160 mA/mm on current on a large area 1" Synoptics™ insulating substrate. A ~170nm Si-doped β-Ga_2O_3 channel with an electron concentration of ~3 x 10^{17} cm^{-3} was grown via metalorganic chemical vapor deposition (MOCVD) on a 1" Fe-doped (010) bulk substrate which was subjected to a 30min HF treatment prior to growth. The growth was done using Agnitron Technology's Agilis 700 MOVPE reactor with TEGa, O_2, and Disilane (Si_2H_6) as precursors with Ar as the carrier gas. A ~210nm unintentionally doped (UID) buffer layer was grown on top of the substrate. The source and drain ohmic contacts were selectively regrown and patterned with a BCl_3 Reactive Ion Etch (RIE) and HCl wet clean. n^+ β-Ga_2O_3 was then grown via MOCVD using Silane (SiH_4) as the silicon precursor and a Ti/Au/Ni Ohmic metal stack was deposited on the regrown regions. A 30nm Al_2O_3 gate dielectric was deposited via ALD at 300C. Lastly, a Ni/Au/Ni gate metal was deposited. The channel sheet charge was measured to be uniform across the wafer (4.6 x 10^{12} cm^{-2} ± 0.6 x 10^{12} cm^{-2}), estimated from the MOSCAP C-V characterization (V_{GS} of +10V (accumulation) to pinch-off). The output and transfer characteristics were measured across the wafer for devices with 1/1.5/1 µm $L_{GS}/L_G/L_{GD}$ dimensions. The pinch-off voltage had a large variation across the wafer (-30 ± 15V). The apparent charge profile from the C-V curves indicates the presence of a parasitic channel at the substrate-epilayer interface which is distributed non-uniformly across the wafer. The on-current (I_D) measured across the wafer was more uniform about 140 ± 20 mA/mm (V_{GS} = +10 V, V_{DS} = 15 V). CV measurements and transfer characteristics indicate a significant density of slow traps (negatively charged) at the dielectric/semiconductor interface, leading to a repeatable shift in the transfer curve from the 2nd scan onward. The MOSFET devices were measured without any field plating or passivation in Fluorinert and the three-terminal destructive breakdown voltages for 5µm and 20µm L_{GD} were 0.65 and 2.1 kV, respectively. Demonstration of wafer-scale growth, processing, and characterization of MOSFETs on a domestic bulk substrate platform reported here is a key step highlighting the technological potential of beta-Gallium Oxide. Acknowledgments: We acknowledge funding from II-VI Foundation, UES Inc. and discussions with AFRL.

3:15pm **EP+HM+MD-MoA-7 Modelling of Impedance Dispersion in Lateral β-Ga_2O_3 MOSFETs Due to Parallel Conductive Si-Accumulation Layer**, ***Zequan Chen***, *A. Mishra, A. Bhat, M. Smith, M. Uren,* University of Bristol, UK*; S. Kumar, M. Higashiwaki,* National Institute of Information and Communications Technology, Japan*; M. Kuball,* University of Bristol, UK

Off-state leakage currents in lateral β-Ga_2O_3 FET devices have previously been attributed to the presence of unintentional Si (n-type) at the interface between epitaxial layer and the substrate[1-5], i.e. a parallel leakage conducting channel. Fe-doping (>$10^{19}$$cm^{-3}$) near the surface of the β-Ga_2O_3 substrate, followed by thermal annealing, has been proven to compensate the unintentional Si impurities, to some degree, thereby reducing leakage current in devices; however, elevated off-state currents and low on-off ratios are still observed in these devices[5]. This work is to provide an analytical model to describe the observed device frequency dispersion due to parallel conductive Si-accumulation layers. Particularly, the dispersion is not associated with active traps as generally believed[6-8].

Lateral β-Ga_2O_3 transistors here were processed on a MBE-grown epitaxial layer on Fe-surface-implanted semi-insulating β-Ga_2O_3 substrates, followed by thermal annealing[5](Fig.1). The transfer characteristics of the device (Fig.2) reveals a large off-state leakage drain current (10^{-6}A/mm) and a small gate leakage current (10^{-12}A/mm). The gate-source capacitance-voltage (C_{GS}) and equivalent conductance-voltage (G_{GS}) profiles between 1kHz and 1MHz (Fig.3) reveal a background dispersion with frequency that is nearly independent of applied gate bias.

An equivalent circuit model is built for explaining impedance dispersion (Fig.4). The parallel leakage path along the entire UID/substrate interface due to Si contaminants provides a coupling path between channels and the probe pads, which are included in the analysis of the device. Therefore, the total capacitance (C_{GS}) will be the "ideal" capacitance (C_{ideal}) superimposed by the contributions from the capacitance and resistance underneath the gate pad(C_{GP}, R_1, C_1), the resistance of the parallel leakage path (R_s), and the capacitance and resistance under the channel (R_2, C_2). Utilizing this model, the measured C_{GS} and G_{GS} are well fitted (Fig.5). The exclusion of traps in the model indicates parallel coupling, instead of traps, should predominantly account for observed frequency dispersion. Moreover, from the extracted R_s in Table.1, the Si concentration at epi/substrate interface is estimated around 1×$10^{18}$$cm^{-3}$, which agrees with that measured from SIMS (Fig.1). This work provides an understanding of the electrical impact of the parallel leakage path of β-Ga_2O_3 devices at moderate frequencies. The signal generated by the parallel leakage can mislead impedance measurements, affecting further analysis such as D_{it} extraction in β-Ga_2O_3 MOSFETs.

Heterogeneous Material Integration
Room Bansal Atrium - Session HM-MoP

Heterogeneous Material Integration Poster Session I

HM-MoP-1 Characterization of Sputtered P-Type Nickel Oxide for Ga_2O_3 Devices, ***Joseph Spencer,*** Naval Research Laboratory*; Y. Ma, B. Wang, M. Xiao,* Virginia Tech*; A. Jacobs, J. Hajzus,* Naval Research Laboratory*; A. Mock,* Weber State University*; T. Anderson, K. Hobart,* Naval Research Laboratory*; Y. Zhang,* Virginia Tech*; M. Tadjer,* Naval Research Laboratory

β-Ga_2O_3 is a promising UWBG (E_G = 4.8 eV) material in the field of power electronics. However, the flat valence band of β-Ga_2O_3 has prevented the realization of p-Ga_2O_3. Without shallow acceptor dopants and p-type conductivity in β-Ga_2O_3, the ability to fabricate high power homojunction devices (PN and JBS diodes) with appropriate field mitigation (guard rings, JTE) is not possible. While other WBG materials such as SiC and GaN can be doped to form p-type conductivity, Ga_2O_3 must rely on a heterojunction. A heterojunction device often exhibits interface traps that negatively impact device performance.

Nickel Oxide (NiO) is a cubic WBG (3.7 eV) p-type semiconductor [1] that is stable at room temperature and forms a favorable band offset to Ga_2O_3 [2]. Reactive ion sputtering is often used to deposit NiO thin films on Ga_2O_3; in our case, a NiO target was utilized to sputter at room temperature. Small changes in sputtering conditions and parameters such as deposition power and pressure, results in widely varying electrical and material properties of the NiO thin films, making characterization challenging. While accurate and repeatable values of N_A can be challenging, a better understand is crucial for device fabrication.

In this work we characterized room-temperature sputtered NiO thin films using electrical methods, ellipsometry, and X-ray photoelectron spectroscopy (XPS) in an attempt to understand the properties of the films. Variations in sputtering power, pressure, and oxygen partial pressure resulted in wide ranging electrical parameters. Most deposition conditions (Table I) result in low mobility (~1 $cm^2/(V \cdot s)$ and high sheet resistance (kΩ/sq – MΩ/sq) making Hall effect characterization difficult. Instead, we used Hg probe CV measurements to estimate free hole concentration ($p=N_A$), a critical parameter for device design (Fig 1). MOS capacitance structures and Hg probe CV show N_A values ranging over two order of magnitude (10^{17}-10^{19} cm^{-3}) stemming from variations in the oxygen partial pressure. As more oxygen is forced into the NiO, the amount of nickel vacancies (Ni^{3+}); the source of p-type conductivity, increases (Table 1). Other methods of NiO film characterization include ellipsometry and XPS. Ellipsometry is critical for investigating film quality, thickness, and band gap; while XPS has been used to observe the content of the Ni vacancies. We have also investigated ohmic contacts to NiO such as Ni, Pt, and PtOx (Fig. 2, Table 2), all of which produce Schottky contacts to Ga_2O_3. While p-type Ga_2O_3 remains unrealized, continued material research into NiO is critical for the advancement of Ga_2O_3 devices.

Heterogeneous Material Integration
Room Bansal Atrium - Session HM-TuP

Heterogeneous Material Integration Poster Session II

HM-TuP-1 Bond-and-Thin Process for Making Heterogeneous Substrate with a Thin Ga_2O_3 Layer om Polycrystalline SiC Substrate, ***Alex Usenko***, *A. Caruso,* University of Missouri-Kansas City*; S. Bellinger,* Semiconductor Power Technologies

Making Power Semiconductor Devices on starting heterogeneous engineered substrates gives numerical advantages over making them on bulk blanket wafers.

For β-Ga_2O_3 it allows to mitigate its critical disadvantage – low thermal conductivity that heavily limits its applications to power semiconductor devices.

In our process flow, we bond 100 mm cmmercially available polycrystalline SiC wafer to 100 mm commercially available β-Ga_2O_3 wafer using room temperarature surface activation bonding process. Then we thin the initial β-Ga_2O_3 to a mnimum thickness needed for desired device voltage.

As each micron of β-Ga_2O_3 withstand up to 800V, the typical final thickness is several microns.

Using polycrystalline SiC substate is for 2 reasons - it is more than 10X cheaper than single crystalline one, and it can have 100X lower electricall resistance compared to aregular nitrogen doped SiC. Indeed, the substrate here is just mechanical support and electrical contact, no semiconductor properties needed. For processes based on epitaxial growth - crystalline lattice is needed, while our process - wafer bonding - is independent on crystal structure.

Next we etch the continuous β-Ga_2O_3 layer into islands equal in shape and area to future power chips to be made on them. Reason is, the continuous layer will not withstand ~1000C processing steps for making MOSFETS and even Schottky diodes. The continuous layer breaks due to difference in thermal expansion. While the islands withstand the thermal processing. The process is being patented.

HM-TuP-3 Design of 10 kV P-Diamond/I-Ga_2O_3/N-Ga_2O_3 Power PN Diodes, ***Hunter Ellis***, *K. Fu,* Department of Electrical and Computer Engineering, University of Utah

β-Ga_2O_3 is a promising ultra-wide bandgap semiconductor material with a unique combination of ultra-wide bandgap, high breakdown field, and large wafer size [1]. Devices based on β-Ga_2O_3 are expected to be smaller, cheaper, more efficient, and more temperature- and power-resistant than other semiconductors [1,2]. However, several obstacles stop β-Ga_2O_3 from being a mainstream electronics material. Specifically, the lack of effective P-type dopants and low thermal conductivity pose significant challenges [1,3]. Since a PN junction is the basic building block for device design, the absence of P-type β-Ga_2O_3 has prevented the full exploitation of its properties, and conventional device design strategies used for Si cannot be transferred to β-Ga_2O_3. On the other hand, high thermal conductivity is critical in electronic devices to minimize heat damage and reduce the likelihood of failure [1, 3].

A P-type diamond and N-type Ga_2O_3 PN heterostructure could address these issues. Diamond could form an ideal heterojunction with β-Ga_2O_3 due to their ultra-wide bandgaps. Diamond is relatively easy to make P-type and has high thermal conductivity; a simulated PN junction is shown in the supplemental document [3,4]. This structure can simultaneously address both problems. However, significant work in device design and integration of epitaxial growth is needed to realize this concept.

In this study, we established a model for the PN heterojunction. We investigated the energy band diagram for the P-diamond/I-Ga_2O_3/N-Ga_2O_3 structure, edge termination to mitigate electric field crowding, drift layer design (I-Ga_2O_3) to increase the breakdown voltage and reduce the on-resistance, and temperature dependence. We successfully designed 10 kV P-diamond/I-Ga_2O_3/N-Ga_2O_3 power PN diodes, and the results are very promising for this type of ultra-wide bandgap PN heterojunction. Effects of interface states on device performance were also investigated due to the importance of epitaxial growth.

[1] A. J. Green *et al.*, "β-Gallium oxide power electronics," *APL Materials,* vol. 10, no. 2, p. 029201, 2022.

[2] Y. Yuan *et al.*, "Toward emerging gallium oxide semiconductors: A roadmap," *Fundamental Research, vol. 1, no. 6, pp. 697-716, Nov. 2021*

[3] S. Pearton *et al.*, "A review of Ga_2O_3 materials, processing, and devices," *Applied Physics Reviews,* vol. 5, no. 1, p. 011301, 2018.

[4] P. Sittimart, S. Ohmagari, T. Matsumae, H. Umezawa, and T. Yoshitake, "Diamond/β-Ga_2O_3 pn heterojunction diodes fabricated by low-temperature direct-bonding," *AIP Advances,* vol. 11, no. 10, p. 105114, 2021.

HM-TuP-5 Heterogeneous Material Integration, ***Yash Mirchandani***, Syrnatec

The use of UWBGs (Ultra-Wide Bandgap Semiconductors) based power converters is an emerging technology that will revolutionize power electronics industries.Space-rated DC-DC converters' performance and power density are primarily limited by high-power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). Power MOSFETs are very susceptible to damage and degradation from the irradiation found in space, especially ionizing radiation. As a response to the current technology gap, Syrnatec in collaboration with University at Buffalo has developed a revolutionary Ga2O3 technology-based UWBGs. These Ga2O3 MOSFETs are capable of demonstrating more robustness to single event effects than their rad-hard power MOSFET counterparts. Because Ga2O3 MOSFETs do not have a metal oxide layer, they are very robust to ionizing radiation, which prevents charge entrapment from TID in high radiation environments. After exposure to 500 krad (Si) ionizing doses, early radiation tests on first generation Ga2O3 MOSFETs showed less than 4% threshold voltage variation (VTH) and less than 3% RDSON change. When the devices were in the OFF state, higher variation was reported (18% VTH and 8% RDSON). In second generation Ga2O3 MOSFETs, no performance degradation has been observed from TID to 1.0 Mrad (Si).Syrnatec's Gallium Oxide MOSFET, an upcoming wide bandgap material that is not only inherently radiation tolerant, but is also suitable for operating in environments with extreme temperatures such as lunar night, where the temperature changes from -153 degrees Celsius to 123 degrees Celsius , and -125 degrees Celsius to 80 degrees Celsius.

Syrnatec will incorporated its Ga2O3 technology into DC-DC converters with a bulk voltage of 20% to 80% and a trickle voltage of above 80%. With a maximum and minimum bulk charge timer (validated as the charge parameters), a Trickle voltage per cell (to be 2V), Boost and trickle voltage settings (Boost is 120% of the rated voltage, Trickle is 2V) and a Device switch off setting (tested on a battery under 20%). With no errors in over voltage and over current test conditions at 150% rated input for 1 sec out of every 10 seconds while maintaining an average of 100% overall rated values for the other 9 seconds. In addition, we have evaluated the success of fault detection across the entire Military Grade Temperature flow. In both buck and boost modes, power conversion efficiency exceeded 96% over the entire temperature range.

Overall, Ga2O3 based power converters can bring several novel features to the US commercial market, including high breakdown voltage, high thermal conductivity, wide bandgap, and low cost.

HM-TuP-6 Si/Ga_2O_3 and GaAsP/Ga_2O_3 P-N Diodes via Semiconductor Grafting, *J. Zhou, D. Kim, H. Jang, Q. Lin,* ***Jiarui Gong***, University of Wisconsin - Madison*; F. Alema, A. Osinsky,* Agnitron Technology Inc.*; K. Chabak, G. Jessen,* Air Force Research Laboratory*; S. Pasayat,* University of Wisconsin - Madison*; C. Cheung, V. Gambin,* Northrop Grumann*; C. Gupta, Z. Ma,* University of Wisconsin - Madison

Ga_2O_3, an ultrawide-bandgap semiconductor, has attracted substantial attention in recent years due to its exceptional electronic properties and its vast potential in power electronics and solar-blind optoelectronics [1]. Despite these attractive properties of Ga_2O_3, there are some challenges to be addressed. For instance, the long-standing issue of lack of p-type doping in Ga_2O_3 has persisted [2]. The inefficiency stems from high ionization energy of acceptors when using the common dopants in Ga_2O_3. As a result, the design and fabrication of high-performance bipolar Ga_2O_3 devices, such as p-n diodes, and HBTs, are still in the research and development stage.

Semiconductor grafting [3], which enables the formation of heterostructures between two arbitrary monocrystalline semiconductors, could be the approach to overcoming the current constraints through the creation of Ga_2O_3 heterostructures, wherein a foreign semiconductor with good p-type doping to integrate with Ga_2O_3 at the atomic level. In this approach, an ultrathin oxide (UO) layer at sub-nanometer scale serves both as the interfacial passivation layer and an effective quantum tunneling layer. In the present case, the surface Ga_2O_3 layer and the possible native oxide of Si should have played the role of the UO layer in the grafting approach.

Employing the semiconductor grafting technology, two types of Ga_2O_3 heterojunctions are created, including Si/Ga_2O_3 and GaAsP/Ga_2O_3, to address the current challenges of ineffective p-type doping in Ga_2O_3 and lack of bipolar devices. In these two structures, p-type Si and p-type GaAsP nanomembranes (NM) are released from their respective epi substrates, transfer-printed and then subsequently chemically bonded to the n-type Ga_2O_3 substrates, forming PN abrupt heterojunctions, and the grafted heterostructures were subsequently fabricated into PN diodes. Their respective diode schematics are shown in Figs. 1 (a) and (b), with preliminary I-V curves for both diodes displayed in Figs. 1 (c) and (d). Both Si/Ga_2O_3 and GaAsP/Ga_2O_3 exhibit excellent rectifying behaviors with rectification ratios of 10^7 and 10^3 at ±2V, respectively. Meanwhile, their ideality factors are characterized to be 1.13 for Si/Ga_2O_3 diode and 1.35 for GaAsP/Ga_2O_3 diode.

In conclusion, we have demonstrated the feasibility to fabricate Ga_2O_3 bipolar devices via the semiconductor grafting approach. The demonstration of the high-performance Si/Ga_2O_3 and GaAsP/Ga_2O_3 PN diodes could lead to functional Ga_2O_3 HBTs in the near future.

References:

[1] M. Higashiwaki *et al. (2016). Semi. Sci. and Tech.*

[2] E. Chikoidze *et al. (2017). Materials Today Physics*

[3] Liu et al. *(2018). arXiv:1812.10225.*

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