Electronic and Photonic Devices, Circuits and Applications
Room Davis Hall 101 - Session EP+HM+MD-MoA

Processes/Devices I
Moderator: Yuhao Zhang, Virginia Tech

1:45pm **EP+HM+MD-MoA-1 Gallium Oxide – Heterogenous Integration with Diamond for Advanced Device Structures**, *H. Kim, A. Bhat, A. Nandi, V. Charan, I. Sanyal, A. Mishra, Z. Abdallah, M. Smith, J. Pomeroy, D. Cherns,* ***Martin Kuball,*** University of Bristol, UK **INVITED**

Potentials for heterogenous integration of Ga_2O_3 with high thermal conductivity materials such as diamond for enabling energy-efficient kV-class power devices are being discussed. The integration alleviates Ga_2O_3 material drawbacks such as its low thermal conductivity and inefficient hole conductivity. The benefits of heterogeneous integration are for example demonstrated through electrical and thermal simulations of a Ga_2O_3-Al_2O_3-diamond superjunction based Schottky barrier diode. The simulation studies show that the novel device has potential to break the R_{ON}-breakdown voltage limit of Ga_2O_3, while showing relatively low rise in temperature compared to conventional devices. As step into their realization, experimental Al_2O_3 assessment namely ledge features in the capacitance-voltage (CV) profiles of Ga_2O_3 metal-oxide-semiconductor (MOS) capacitors were investigated using UV-assisted CV measurements; an interface trapping model is presented whereby the capacitance ledge is associated with carrier trapping in deep-level states at the Al_2O_3/Ga_2O_3 interface. Trench-Schottky Barrier diodes with breakdown voltage in excess of 1.5kV were demonstrated. First steps for the materials integration of Ga_2O_3 with diamond towards a superjunction based trench-Schottky barrier diode, including epitaxial growth of Ga_2O_3 on single crystal diamond substrates are being reported.

2:15pm **EP+HM+MD-MoA-3 Highly Scaled β-Ga2O3 MOSFET with 5.4 MV/cm Average Breakdown Field and Near 50 GHz fMAX**, ***Chinmoy Nath Saha,*** *A. vaidya,* SUNY at Buffalo*; A. Bhuiyan, L. Meng,* Ohio State University*; S. Sharma,* SUNY at Buffalo*; H. Zhao,* Ohio State University*; U. Singisetti,* SUNY at Buffalo

This letter reports the high performance β-Ga2O3 thin channel MOSFET with T gate and degenerately doped source/drain contacts regrown by Metal Organic Chemical Vapour Deposition (MOCVD). Device epitaxial layer was grown by Ozone MBE. Highly scaled T-gate (LG=160-200 nm) was fabricated to achieve enhanced RF performance and passivated with 200 nm Silicon Nitride (Si3N4). Peak drain current (ID,MAX) of 285 mA/mm and peak trans-conductance (gm) of 52 mS/mm were measured at 10 V drain bias with 23.5 Ω mm on resistance (Ron). Metal/n+ contact resistance of 0.078 Ω mm was extracted from Transfer Length Measurements (TLM). Channel sheet resistance was measured to be 14.2 Kiloohm/square from cross bar structure. Based on TLM and cross bar measurements, we determined that on resistance (Ron) is possibly dominated by interface resistance between channel and regrown layer. Different growth methods originating from MBE channel layer and MOCVD regrown n++ layer can cause this high interface resistance. A gate-to-drain breakdown voltage(V_{DG}) of 192 V is measured for L_{GD}= 355 nm resulting in average breakdown field (E_{AVG}) of 5.4 MV/cm. This $E_{AVG}$is the highest reported among all sub-micron gate length lateral FETs. And highest overall without using any intentional field plate techniques. Current gain cut off frequency (f_T) of 11 GHz and record power gain cut off frequency (f_{MAX}) of approximately 48 GHz were extracted from small signal measurements. f_T is possibly limited by DC-RF dispersion due to interface traps which need further investigation. We observed moderate DC-RF dispersion at 200 ns pulse width (for both output and transfer curve) which can corroborate our theory. We recorded f_T.V_{BR} product of 2.112 THz.V for 192 V breakdown voltage which is similar to GaN HEMT devices. Our device surpasses the switching figure of merit of Silicon because of low on resistance and high breakdown voltage, and competitive with mature wide-band gap devices. Proper surface cleaning between channel and regrowth layer and sub-100 nm T gate device structure can pave the way for better RF performance.

2:30pm **EP+HM+MD-MoA-4 Demonstration of a β-Ga_2O_3 Lateral Diode Full-Wave Rectifier Monolithic Integrated Circuit**, ***Jeremiah Williams,*** *J. Piel, A. Islam, N. Hendricks, D. Dryden, N. Moser,* Air Force Research Laboratory, Sensors Directorate*; W. Wang,* Wright State University*; K. Liddy, M. Ngo,* Air Force Research Laboratory, Sensors Directorate*; N. Sepelak,* KBR Inc.*; A. Green,* Air Force Research Laboratory, Sensors Directorate

Beta Gallium Oxide (Ga_2O_3) is well positioned excel in high power density applications due to its wide band gap, critical field strength, multiple shallow donor species, and melt grown native substrates. Monolithic integrated circuits (ICs) can advance Ga_2O_3 by reducing the size, weight, and connectivity parasitics of components. Lateral topologies with thin epitaxy on insulating substrates enable simple fabrication and integration of RF components. This work utilizes this system to demonstrate a fundamental circuit, the diode full-wave rectifier, with an accompanying design study of the interdigitated lateral diode topology.

The devices (Fig. 1) are fabricated from a 65 nm Si-doped Ga_2O_3 epitaxial layer grown by MBE on a Fe-doped Ga_2O_3 substrate. Epitaxy carrier concentration is measured to be 2×10^{18} cm^{-3} from C-V test structures (Fig. 2). The cathode is a Ti/Al/Ni/Au Ohmic contact annealed at 470 °C. The devices are isolated with a BCl_3 ICP mesa etch. A field-plate and surface passivation oxide of 80 nm thick Al_2O_3 is deposited by ALD. The anode is a Ni/Au Schottky contact. A full-wave rectifier and 16 diode variations are evaluated. The diodes have square and rounded contacts; anode finger counts of 1, 2, 4, and 8; and anode-cathode lengths ($L_{A\text{-}C}$) of 5, 7, and 12 µm. Anode length is 4 µm and width is 48 µm. The diodes in the rectifier have round contacts, 4 anode fingers, and 12 µm $L_{A\text{-}C}$ (Fig. 3). The rectifier is measured on-chip with micro probes. An AC signal is generated with a high-voltage amplifier and measured on an oscilloscope. The output of the rectifier to a 47 kΩ load is measured differentially, using a voltage divider to protect the oscilloscope from voltage spikes (Fig. 4).

The rectifier successfully demonstrates full-wave rectification of sine waves up to 144 V_{rms} (205 V peak) and 400 Hz (Fig. 5). The rectifier demonstrates 83 % efficiency and 0.78 W peak power. To the authors' knowledge, this is the first demonstration of a diode full-waver rectifier IC in Ga_2O_3. From the lateral diode design study, rounded contacts improve the average breakdown voltage (V_{bk}) by 20% (+41 V) without effecting specific on-resistance ($R\text{-}_{on,sp}$) (Fig. 6). The number of anode fingers does not statistically affect V_{bk}, and improves average $R\text{-}_{on,sp}$ by 18% (-0.45 mΩ-cm^2) at eight (Fig. 7). Scaling $L_{A\text{-}C}$ to 5, 7, and 12 µm also scales average $R_{on,sp}$ to 2.0, 2.9, and 8.6 mΩ-cm^2. Average V_{bk} scales as well, but with no change between 5 and 7 µm $L_{A\text{-}C}$ (248, 242, and 341 V) (Fig. 8). The J-V characteristics of a single diode (round contacts, eight fingers, 5 µm $L_{A\text{-}C}$) are included in Fig. 9.

2:45pm **EP+HM+MD-MoA-5 Improved Breakdown Strength of Lateral β-Ga_2O_3 MOSFETs Using Aerosol-Spray-Printed hBN-BCB Composite Encapsulation**, ***Daniel Dryden,*** Air Force Research Laboratory, Sensors Directorate*; L. Davidson,* KBR, Inc.*; K. Liddy, J. Williams, T. Pandhi, A. Islam, N. Hendricks, J. Piel,* Air Force Research Laboratory, Sensors Directorate*; N. Sepelak,* KBR, Inc.*; D. Walker, Jr., K. Leedy,* Air Force Research Laboratory, Sensors Directorate*; T. Asel, S. Mou,* Air Force Research Laboratory, Materials and Manufacturing Directorate, USA*; F. Ouchen,* KBR, Inc.*; E. Heckman, A. Green,* Air Force Research Laboratory, Sensors Directorate

Beta gallium oxide (β-Ga_2O_3) has shown promise for high-voltage power devices and power switching due to its large critical field strength E_c estimated at 8 MV/cm [1]. Dielectric passivation and testing under Fluorinert immersion [2] are used to increase breakdown voltage V_{bk} and avoid air breakdown, respectively, with the highest V_{bk} lateral Ga_2O_3 devices using polymer passivation [3]. The polymer benzocyclobutene (BCB) exhibits high dielectric strength, low parasitics, and good manufacturability [4,5]. It may be loaded with hexagonal boron nitride (hBN), improving thermal conductivity, dielectric response, and mechanical durability [6]. Coatings can be applied via aerosol jet printing, allowing multiple experimental conditions across devices on a single sample. Here, lateral β-Ga_2O_3 MOSFETs encapsulated with hBN-loaded BCB (hBN-BCB) which exhibit significantly enhanced V_{bk} compared to devices encapsulated with BCB alone or without encapsulation.

Si-doped β-Ga_2O_3 was grown epitaxially on a semi-insulating, Fe-doped (010) Ga_2O_3 substrate via molecular beam epitaxy to a nominal thickness of 65 nm and a doping of $2.8\text{+-}0.2\text{x}10^{17}$ cm^{-3}. Ti/Al/Ni/Au ohmic contacts were deposited and annealed at 470 °C for 60 s in N_2. Ni/Au gates were deposited on a gate oxide of 20 nm Al_2O_3, followed by a passivation oxide of 85 nm Al_2O_3. Thick Au contacts were formed using evaporation and electroplating. Devices with BCB or hBN-BCB were encapsulated using an

Optomec AJ200 aerosol jet printer. Inks consisted of Cyclotene 4022-35, cyclohexanone and terpineol, with or without hBN.

V_{bk} was tested under air or Fluorinert (Figure 2). Devices tested under Fluorinert, BCB, and BCB plus Fluorinert showed a 1.7x improvement in V_{bk} over air. Devices with hBN-BCB showed an improvement of 3.7x over air and 1.35x over BCB alone. The hBN-BCB-coated devices (N=6) show significant improvement in V_{bk} over the devices coated BCB alone (N=3) with p<0.011 (single-tail heteroscedastic T-Test).

Device performance of the highest-V_{bk} device are shown in Figure 3. The device, before encapsulation, had R_{on} of 683 Ω·mm, I_{max} of 3.42 mA/mm, $G_{m,peak}$ of 1.14 mS/mm, V_{th} of -3.8 V, V_{off} of -6.5 V, and V_{bk} of 951 V ($E_{crit,avg}$ 1.23 MV/cm). Device performance was unaffected by hBN-BCB encapsulation (Fig. 3b) excepting a change in V_{off} to -8 V. No significant gate leakage was observed during device operation or breakdown. Breakdown likely occurred due to peak fields exceeding the E_{crit} of one or more materials at the drain-side edge of the gate. These results provide a significant improvement over existing encapsulation approaches in β-Ga_2O_3 lateral MOSFETs.

3:00pm **EP+HM+MD-MoA-6 Wafer-Scale β-Ga_2O_3 Field Effect Transistors with MOCVD-Grown Channel Layers**, ***Carl Peterson***, University of California Santa Barbara*; F. Alema,* Agnitron Technology Incorporated*; Z. Ling, A. Bhattacharyya,* University of California Santa Barbara*; S. Roy,* University of California at Santa Barbara*; A. Osinsky,* Agnitron Technology Incorporated*; S. Krishnamoorthy,* University of California Santa Barbara

We report on the growth, fabrication, and wafer-scale characterization of lateral high-voltage MOSFETs with ~120-160 mA/mm on current on a large area 1" Synoptics™ insulating substrate. A ~170nm Si-doped β-Ga_2O_3 channel with an electron concentration of ~3 x 10^{17} cm^{-3} was grown via metalorganic chemical vapor deposition (MOCVD) on a 1" Fe-doped (010) bulk substrate which was subjected to a 30min HF treatment prior to growth. The growth was done using Agnitron Technology's Agilis 700 MOVPE reactor with TEGa, O_2, and Disilane (Si_2H_6) as precursors with Ar as the carrier gas. A ~210nm unintentionally doped (UID) buffer layer was grown on top of the substrate. The source and drain ohmic contacts were selectively regrown and patterned with a BCl_3 Reactive Ion Etch (RIE) and HCl wet clean. n^+ β-Ga_2O_3 was then grown via MOCVD using Silane (SiH_4) as the silicon precursor and a Ti/Au/Ni Ohmic metal stack was deposited on the regrown regions. A 30nm Al_2O_3 gate dielectric was deposited via ALD at 300C. Lastly, a Ni/Au/Ni gate metal was deposited. The channel sheet charge was measured to be uniform across the wafer (4.6 x 10^{12} cm^{-2} ± 0.6 x 10^{12} cm^{-2}), estimated from the MOSCAP C-V characterization (V_{GS} of +10V (accumulation) to pinch-off). The output and transfer characteristics were measured across the wafer for devices with 1/1.5/1 µm $L_{GS}/L_G/L_{GD}$ dimensions. The pinch-off voltage had a large variation across the wafer (-30 ± 15V). The apparent charge profile from the C-V curves indicates the presence of a parasitic channel at the substrate-epilayer interface which is distributed non-uniformly across the wafer. The on-current (I_D) measured across the wafer was more uniform about 140 ± 20 mA/mm (V_{GS} = +10 V, V_{DS} = 15 V). CV measurements and transfer characteristics indicate a significant density of slow traps (negatively charged) at the dielectric/semiconductor interface, leading to a repeatable shift in the transfer curve from the 2nd scan onward. The MOSFET devices were measured without any field plating or passivation in Fluorinert and the three-terminal destructive breakdown voltages for 5µm and 20µm L_{GD} were 0.65 and 2.1 kV, respectively. Demonstration of wafer-scale growth, processing, and characterization of MOSFETs on a domestic bulk substrate platform reported here is a key step highlighting the technological potential of beta-Gallium Oxide. Acknowledgments: We acknowledge funding from II-VI Foundation, UES Inc. and discussions with AFRL.

3:15pm **EP+HM+MD-MoA-7 Modelling of Impedance Dispersion in Lateral β-Ga_2O_3 MOSFETs Due to Parallel Conductive Si-Accumulation Layer**, ***Zequan Chen***, *A. Mishra, A. Bhat, M. Smith, M. Uren,* University of Bristol, UK*; S. Kumar, M. Higashiwaki,* National Institute of Information and Communications Technology, Japan*; M. Kuball,* University of Bristol, UK

Off-state leakage currents in lateral β-Ga_2O_3 FET devices have previously been attributed to the presence of unintentional Si (n-type) at the interface between epitaxial layer and the substrate[1-5], i.e. a parallel leakage conducting channel. Fe-doping (>$10^{19}$$cm^{-3}$) near the surface of the β-Ga_2O_3 substrate, followed by thermal annealing, has been proven to compensate the unintentional Si impurities, to some degree, thereby reducing leakage current in devices; however, elevated off-state currents and low on-off ratios are still observed in these devices[5]. This work is to provide an analytical model to describe the observed device frequency dispersion due to parallel conductive Si-accumulation layers. Particularly, the dispersion is not associated with active traps as generally believed[6-8].

Lateral β-Ga_2O_3 transistors here were processed on a MBE-grown epitaxial layer on Fe-surface-implanted semi-insulating β-Ga_2O_3 substrates, followed by thermal annealing[5](Fig.1). The transfer characteristics of the device (Fig.2) reveals a large off-state leakage drain current (10^{-6}A/mm) and a small gate leakage current (10^{-12}A/mm). The gate-source capacitance-voltage (C_{GS}) and equivalent conductance-voltage (G_{GS}) profiles between 1kHz and 1MHz (Fig.3) reveal a background dispersion with frequency that is nearly independent of applied gate bias.

An equivalent circuit model is built for explaining impedance dispersion (Fig.4). The parallel leakage path along the entire UID/substrate interface due to Si contaminants provides a coupling path between channels and the probe pads, which are included in the analysis of the device. Therefore, the total capacitance (C_{GS}) will be the "ideal" capacitance (C_{ideal}) superimposed by the contributions from the capacitance and resistance underneath the gate pad(C_{GP}, R_1, C_1), the resistance of the parallel leakage path (R_s), and the capacitance and resistance under the channel (R_2, C_2). Utilizing this model, the measured C_{GS} and G_{GS} are well fitted (Fig.5). The exclusion of traps in the model indicates parallel coupling, instead of traps, should predominantly account for observed frequency dispersion. Moreover, from the extracted R_s in Table.1, the Si concentration at epi/substrate interface is estimated around 1×$10^{18}$$cm^{-3}$, which agrees with that measured from SIMS (Fig.1). This work provides an understanding of the electrical impact of the parallel leakage path of β-Ga_2O_3 devices at moderate frequencies. The signal generated by the parallel leakage can mislead impedance measurements, affecting further analysis such as D_{it} extraction in β-Ga_2O_3 MOSFETs.

Electronic and Photonic Devices, Circuits and Applications Room Bansal Atrium - Session EP-MoP

Electronic and Photonic Devices, Circuits and Applications Poster Session I

EP-MoP-2 Anisotropy Nature of NiO_x/β-Ga_2O_3*p-n* Heterojunctions on (-201), (001), and (010) β-Ga_2O_3 Substrates, ***Dinusha Herath Mudiyanselage***, *D. Wang, H. Fu,* Arizona State University

Recently, β-Ga_2O_3 has been extensively studied for power, optical, and RF electronics due to its large bandgap of 4.9 eV and high breakdown field of 8 MV/cm. However, most of the demonstrated devices are unipolar due to the lack of *p*-type Ga_2O_3, such as FETs and SBDs. This is primarily attributed to the absence of shallow acceptors in Ga_2O_3. As a solution, other *p*-type materials, such as NiO_x, have been utilized to produce β-Ga_2O_3 based *p-n* heterojunctions. Several NiO_x/β-Ga_2O_3 devices, such as *p-n* diodes and junction barrier Schottky diodes, have been demonstrated with excellent electrical properties. Moreover, due to its highly asymmetric monoclinic crystal structure, β-Ga_2O_3 exhibits anisotropic properties along different crystal orientations. However, the impacts of different β-Ga_2O_3 crystal orientations on NiO_x/β-Ga_2O_3*p-n* heterojunction are still unclear. In this work, we perform a systematic study of NiO_x/β-Ga_2O_3*p-n* heterojunctions on (-201), (001), and (010) crystal orientations. The EFG-grown β-Ga_2O_3 substrates were acquired with a similar *n*-type doping concentration and thickness. First, the substrates were cleaned using acetone, IPA, and DI water. The Ti/Au (20/130 nm) back contacts were deposited by E-beam evaporation followed by rapid thermal annealing at 500 °C in N_2. Then, standard photolithography was performed to define patterns for deposition of NiO_x and the anode. 200 nm NiO_x and the anode Ni/Ti/Au (20/15/100 nm) were deposited using E-beam evaporation, followed by a liftoff process to isolate devices. I-V and C-V measurements were performed using a 4200 SCS semiconductor parameter analyzer. All devices show an excellent rectification with on/off ratio >10^9. I-V measurements indicate a turn-on voltage of 2.09, 2.22, and 2.50 V, an ideality factor of 1.95, 2.03, and 2.13, and an on-resistance of 2.92, 1.55, and 6.50 mΩ.cm^2 for (-201), (001), and (010) devices, respectively. C-*f* measurements indicated an interface state density of 4.3 × 10^{10}, 7.4 × 10^{10}, and 1.6 × 10^{11} $eV^{-1}cm^{-2}$ for (-201), (001), and (010) plane devices, respectively. Furthermore, the reverse recovery of the diodes shows a slight difference between (-201) [or (001)] and (010) devices due to the anisotropic nature of β-Ga_2O_3. These differences in the electrical properties are attributed to the different atomic configurations, the density of dangling bonds, and conductivity-modulated hole injection into β-Ga_2O_3. Further investigation through temperature-dependent measurements will reveal more information about the anisotropic nature of NiO_x/β-Ga_2O_3*p-n* heterojunctions.

EP-MoP-3 Ultrathin Films of Amorphous Gallium Oxide for Ultra-Fast Solar-Blind Photodetectors, ***Damanpreet Kaur***, *M. Kumar,* Indian Institute of Technology Ropar, India

In addition to stable and meta-stable crystalline phases of Ga_2O_3, its amorphous phase is also being explored for various applications owing to its technological advantage like room temperature and large area growth for next generation solar-blind photodetectors .[1] But being often sub-stoichiometric and replete with oxygen vacancies, performance of amorphous thin film PDs is far below their crystalline counterparts. Hence, novel methods and techniques need to be adopted to improve performance of such devices.[2] Herein, we report one such method where ultra-thin films of amorphous Ga_2O_3 are deposited on nanopatterned SiO_2 coated Si substrate. Controlled nanopatterns or ripple formation is carried out by irradiating SiO_2/Si substrate with 500eV Ar^+ ions for variable times. Morphology of ripples formed on substrate is studied using AFM images to calculate the characteristic wavelength and Power Spectral Density. Amorphous Ga_2O_3 (~5nm) is then sputtered onto these rippled substrates using RF Magnetron Sputtering at room temperature. Uniformity of Ga_2O_3 is confirmed by EDX elemental mapping studies. Reflectance measurements were carried out using UV-Vis spectroscopy and results showed lower reflectance as compared to non-rippled because of the enhanced absorption due to multiple scattering by the substrate and enhanced surface area. FDTD was used to simulate reflectance measurements which are well in agreement with experimental results.

The performance of subsequently fabricated photodetectors showed that conformally coated devices had an enhanced performance as compared to non-rippled “bare” device. The solar-blind PDs show an increase in the responsivity from ~3 mA $W^{-1}$to 433 mA W^{-1} – an increment of more than 140 times at +5V. For the response times, bare device shows slow rise/fall time of 0.37s /0.39s whereas the conformal devices showed an ultrafast rise time of 896µs and fall time of 710µs, respectively, to 254 nm incident light. The detailed analysis showed that the device performance can be attributed to the incorporation of elemental Si from the substrate below, the presence of which is confirmed by XPS. This study shows how amorphous Ga_2O_3 films can be used to fabricate ultra-fast devices, especially for next-generation solar-blind PD applications.

References:

1. Kaur, D. and M. Kumar, *A Strategic Review on Gallium Oxide Based Deep-Ultraviolet Photodetectors: Recent Progress and Future Prospects.* Advanced Optical Materials, 2021. **9**(9): p. 2002160.
2. Kaur, D., et al., *Surface nanopatterning of amorphous gallium oxide thin film for enhanced solar-blind photodetection.* Nanotechnology, 2022. **33**(37): p. 375302.

Material and Device Processing and Fabrication Techniques
Room Davis Hall 101 - Session MD+AC+EP-TuA

Process/Devices II

Moderator: Yuhao Zhang, Virginia Tech

3:45pm **MD+AC+EP-TuA-9 Large Area Trench β-Ga_2O_3 Schottky Barrier Diode with Extreme-K Dielectric Resurf***, Saurav Roy, A. Bhattacharyya,* University of California Santa Barbara*; J. Cooke,* University of Utah*; C. Peterson,* University of California Santa Barbara*; B. Rodriguez,* University of Utah*; S. Krishnamoorthy,* University of California Santa Barbara

We report the first combination of high-k dielectric RESURF with trench geometry to realize low reverse leakage large area (1mm^2 and 4mm^2) β-Ga_2O_3 Schottky Barrier Diodes with high current values (15A pulsed, 9A DC). 1.2 µm deep trenches are etched on HVPE-grown 11 µm epilayer with 8×10^{15} cm^{-3} apparent charge density concentration using dry etching and 300 nm $BaTiO_3$. (BTO)is then sputter deposited which is followed by annealing at 700°C to enhance the dielectric constant. The fins are then opened using dry etching. Pt/Au Schottky contacts are deposited using e-beam evaporation with planetary rotation for conformal deposition. To further improve the breakdown voltage field plates are used with Si_3N_4 as the field plate oxide. A planar SBD, a BTO field-plated SBD, and a trench SBD with high-k RESURF are fabricated for comparison. The on resistance ($R_{on,sp}$ normalized to the device footprint) of the planar and field plated SBDs are extracted to be 7.9 and 8.2 mΩ-cm^2, respectively, and an increased on resistance of 10.8 mΩ-cm^{-2} is measured for small area (200×200 μm^2) trench SBD with high-k RESURF, indicating dry etching induced damage. The breakdown voltage of the BTO field-plated SBD increases to 2.1 kV from 816 V (planar SBD) whereas the breakdown voltage increases to 2.8-3kV for the trench SBD with high-k RESURF. A very low leakage current density of 2×10^{-4} A/cm^2 is measured for the trench SBD at 2.8 kV. The 1 mm^2 trench SBD exhibits a current of 3.7A(Pulsed)/2.9A(DC) and the 4mm^2 trench SBD exhibitsa current of 15A(Pulsed)/9A(DC) at 5V. The breakdown (catastrophic) voltage of the 1mm^2 and 4mm^2 trench SBDs are measured to be 1.4 and 1.8kV. The leakage currents at breakdown are significantly lower compared to other high current SBDs reported in the literature despite the large area of the device, due to the much-reduced parallel field at the metal/semiconductor interface. Temperature dependence of on resistance shows lower temperature co-efficient (α = 0.87) which is lower than SiC SBDs. The large area high-k RESURF trench SBDs also has lowest $V_{on}I_{leakage}$ product for any β-Ga_2O_3 SBDs with more than 1kV breakdown voltage and 1A current, which is important to reduce both the on and off-state power dissipation. The 4mm^2 high-k RESURF trench SBD has the highest current (5A(DC)/9A(Pulsed)) at V_F = V_{on}+2V with breakdown voltage more than 1.3kV and exhibits lowest leakage current for similar rated device from literature.

This material is based upon work supported by the II-VI Block Gift Program and the Air Force Office of Scientific Research MURI award FA9550-21-0078.

4:00pm **MD+AC+EP-TuA-10 Fabrication and Characteristics of Ga_2O_3 MOSFET using p-NiO for Normally-off Operation***, Daehwan Chun, Y. Jung, J. Park, J. Hong, N. Joo, T. Kim,* Hyundai Motor Company, Republic of Korea

In order to increase sales of electric vehicles, it is essential to have market competitiveness by reducing price and improving performance, as well as improving mileage. To increase the mileage of an electric vehicle, it is important to efficiently use the limited power of the battery. The inverter/converter/OBC plays a role in converting electrical energy into a form suitable for electrical components, and the power semiconductor performs switching and rectification operations in the components responsible for such power conversion. Therefore, the performance of power semiconductors is directly related to the mileage of electric vehicles.

Existing power semiconductors mainly used Silicon(Si) materials, but recently, Silicon Carbide(SiC) power semiconductors with improved performance have been mass-produced and started to be installed in vehicles. Gallium Oxide(Ga_2O_3), which has a wider energy bandgap(4.7~4.9eV) than SiC, has a high critical electric field, excellent electron transport ability, and high-quality large-area substrate growth, so it has the advantage of not only performance compared to existing GaN or SiC semiconductor but also easy manufacturing process. In particular, the unit price of Ga_2O_3 epitaxial wafer is expected to be reduced to 1/3 of that of SiC. Therefore, the manufacturing cost is also expected to be lower than that of SiC power semiconductors.

In this paper, we present the fabrication results of Ga_2O_3-based lateral MOSFETs for inverter/converter/OBC applications of electric vehicles. Normally-off operation was secured through the application of NiO, which does not require an ion implantation process, and a breakdown voltage of 600V was achieved. In addition, Al_2O_3 was used as a gate insulating film to suppress gate leakage current, and high-concentration ITO was applied to form an ohmic junction.

Applying NiO to form the depletion layer in the channel region when the MOSFET is off-state ensures normally-off operation of the Ga_2O_3 MOSFET. However, there is a limit to gate voltage application due to leakage current because of the existence of a pn heterojunction diode in the gate region. To solve this problem, an insulating film(Al_2O_3) was formed between NiO and the gate metal. The threshold voltage of the MOSFET with this structure formed a high value of 30V or more, so the threshold voltage was lowered by modifying the concentration of the Ga_2O_3 epitaxial layer. As a result, some drain-source leakage current occurred, but an IV characteristic graph that clearly distinguishes the On/Off state of the MOSFET was obtained.

4:15pm **MD+AC+EP-TuA-11 On the Mg-Diffused Current Blocking Layer for Ga_2O_3 Vertical Diffused Barrier Field-Effect-Transistor (VDBFET)***, Ke Zeng, Z. Bian, S. Chowdhury,* Stanford University

To truly realize the potential of the Ga_2O_3 in a transistor, it is imperative to design a buried gate barrier junction to circumvent the pre-mature breakdown near the gate often seen in lateral structures. Owing to the high diffusivity of dopants and defects in Ga_2O_3, in contrast to that of, for example, SiC at a moderate temperature, we propose the use of diffusion doping as a rapid and non-invasive platform to explore the possibility of an effective current blocking layer (CBL) in vertical Ga_2O_3 transistors. In this work, we will discuss the development and characteristics of the Mg diffused CBL that was recently utilized to demonstrate an efficient Ga_2O_3 VDBFET with remarkable pinch-off characteristics.

The process (Fig. 1) starts with a commercially available Ga_2O_3 HVPE epitaxial wafer. The wafer was first coated with a highly Mg-doped spin-on-glass (SOG) layer which was subsequently cured and then patterned by HF to form the selective Mg dopant source. A thick PECVD layer was deposited onto the sample to isolate and stabilize the diffusion doping process. The Mg was then diffused into the wafer under a 950 °C furnace annealing for ~1 hr to form the CBL. The dopant oxide stack was stripped clean by an HF dip afterward. A Ni/Au anode was then deposited on top of the CBL region for the 2-terminal CV and IV studies shown in Fig. 2. Furthermore, for the 3-terminal VDBFET, a high dose titled Si triple ion implantation was done to form the source contact region inside the CBL area, followed by an activation annealing. The Ti/Au and Ni/Au composite source electrode was deposited on top of the source and CBL region respectively. A Ti/Au drain contact was then deposited on the back of the wafer. A 25nm ALD Al_2O_3 was used as the gate oxide, and a Ti/Ni/Au stack was deposited as the gate contact on top of the wafer.

From a simple CV analysis on the metal-isolation-semiconductor (MIS) structure, it's confirmed that the conductivity of the Ga_2O_3 epitaxial layer was successfully modulated by the Mg diffusion process for a depth of ~ 1.6 µm. The same MIS structure measured a reverse breakdown voltage of 466 V. However, when the surface is further doped with implanted Si^{++} layer, the formed NIN diode only blocks ~72V, the same as the final device blocking voltage. The VDBFET showed amazing transistor characteristics with decent saturation, on-current without any optimization, as well as a current on/off ratio > 10^9. Due to the compensation of electrons by Mg in the gate region, the transistor exhibited enhancement mode operation with a turn-on voltage of ~7V. The breakdown voltage, however, was only measured to be 72 V under a gate bias of 0 V.

4:30pm **MD+AC+EP-TuA-12 Electrical Properties of p-NiO/β-Ga_2O_3 Vertical PN Heterojunction Diode for Power Device Applications***, Youngkyun Jung, D. Chun,* Hyundai Motor Company, Republic of Korea

In this paper, the p-type NiO/β-Ga_2O_3 vertical pn heterojunction diode for power device application was fabricated, and the electrical characteristics of the device was evaluated. The β- Ga_2O_3 has a wide energy bandgap of about 4.8eV, and that is expected to be a material for next-generation power semiconductors with high breakdown voltage and low power loss. Compared to SiC (Silicon carbide) and GaN (Gallium Nitride), which are used as common materials for power semiconductors, it has a breakdown field (8MV/cm) that is about 3 times higher, and Baliga's FOM (3,400), which represents the semiconductor figure of merit, it has a value 4 to 10 times higher than that of GaN and SIC materials. Recently, β-Ga_2O_3 has been fabricated in the form of an epitaxial layer on a wafer and applied to power devices such as MOSFETs, MESFETs, Schottky barrier diodes, and pn

junction diodes. The p-NiO has a wide band gap of 3.6 eV or more, p-type characteristics of NiO generally is induced by nickel vacancies or oxygen interstitials, that are defects provide the hole carriers. The carrier concentrations of p-NiO can be controlled in the range of 10^{16} to 10^{19} cm^{-3} with the amount of oxygen gas during the sputtering deposition process. The depletion region width of p-NiO/β-Ga_2O_3 can be changed according to the change in the carrier concentration of p-NiO. To fabricate the pn vertical heterojunction diode, p-NiO was deposited on the β-Ga_2O_3 epitaxial layer with a thickness of 250nm by using RF magnetron sputtering, and 100 nm of Ni metal for ohmic contact was deposited on the deposited p-NiO by using DC magnetron sputtering. The I-V characteristics of the fabricated pn heterojunction diode were measured by keithley 2410, and the C-V characteristics were measured by Keysight 4284A. As a result of measuring electrical characteristics, the pn heterojunction diode has a lower leakage current value than the previously reported Schottky Barrier Diode, and on/off ratio is about 10^9. When the carrier concentration of deposited p-NiO was $10^{19}cm^{-3}$, the turn-on voltage, current density, Ron value and breakdown voltage values of pn heterojunction diode were shown 2.2V, 242A/cm^2@4V, 17mΩ.cm^2@4V, and –465V respectively.

4:45pm **MD+AC+EP-TuA-13 Effects of Oxygen Reactive Ion Etching and Nitrogen Radical Irradiation on Electrical Properties of Ga_2O_3 Schottky Barrier Diodes**, ***Shota Sato***, *K. Eguchi,* Department of Physics and Electronics, Osaka Metropolitan University, Japan*; Z. Wang,* National Institute of Information and Communications Technology, Japan*; T. Kitada, M. Higashiwaki,* Department of Physics and Electronics, Osaka Metropolitan University, Japan

β-Ga_2O_3 has attracted great attention as a new wide bandgap semiconductor mainly for power devices. Oxygen reactive ion etching (O_2 RIE) is often used to remove a resist and/or an organic contamination in Ga_2O_3 device processing. However, this process usually causes damage to a Ga_2O_3 surface degrading device characteristics. On the other hand, we found that nitrogen (N) radical irradiation can significantly restore the Ga_2O_3 surface damage. In this study, we investigated effects of the O_2 RIE and N radical irradiation on electrical properties of Schottky barrier diodes (SBDs) fabricated on *β*-Ga_2O_3 (100) and (010) substrates.

Ga_2O_3 SBD structures were fabricated using unintentionally doped *β*-Ga_2O_3 (100) and (010) bulk substrates with an effective donor concentration of less than 2×10^{17} cm^{-3}. We evaluated electrical properties of the Ga_2O_3 SBDs fabricated on the substrates treated by four different processes: (a) no surface treatment, (b) O_2 RIE, (c) N radical irradiation, (d) O_2 RIE followed by N radical irradiation. The O_2 RIE was performed at an RF power of 50 W for 90 seconds. The N radical irradiation was conducted using an RF plasma cell in a molecular beam epitaxy growth chamber at a substrate temperature of 700°C and an RF power of 500 W for 2 hours.

We first studied current density–voltage (*J–V*) characteristics of the Ga_2O_3 (100) SBDs processed by the four different methods. In case of the devices with no treatment, a large variation of the turn-on *V* in a wide range of 0.5–1.1 V was observed. The O_2 RIE process further spread the variation to 0.2–1.0 V, indicating that the Ga_2O_3 (100) surface was more damaged. Furthermore, some devices showed kinks in their *J–V* curves. The curves with the kinks look like an overlap of *J–V* characteristics for a few area with different Schottky barrier heights under the anode electrode. In contrast, with and without the O_2 RIE, *J–V* characteristics of both SBDs treated by the N radical irradiation showed an almost constant turn-on *V* of 0.3 V and no kink. These results indicate that the N radical irradiation has effects to significantly restore the Ga_2O_3 surface damage and equalize the surface condition. Qualitatively the same effects of nitridation were confirmed for the Ga_2O_3 (010) SBDs.

In conclusion, we found that N radical irradiation is effective for restoring Ga_2O_3 surface damage, which leads to improvements in electrical properties of the Schottky interface.

This work was supported in part by the Development Program, “Next-Generation Energy-Saving Devices” of the Ministry of Internal Affairs and Communications, Japan (JPMI00316).

Electronic and Photonic Devices, Circuits and Applications Room Bansal Atrium - Session EP-TuP

Electronic and Photonic Devices, Circuits and Applications Poster Session II

EP-TuP-6 Investigating the Properties of β-Ga_2O_3 Schottky Diodes on MOCVD-Grown (001) Drift Layer, ***Prakash P. Sundaram,*** University of Minnesota, USA*; F. Alema, A. Osinsky,* Agnitron Technology*; S. Koester,* University of Minnesota, USA

In this study, we investigate the electrical properties of Schottky barrier diodes (SBD) fabricated on epitaxial layers grown on (001) β-Ga_2O_3 (GOX) by metal-organic chemical vapor deposition (MOCVD). While various growth methods have been used for epitaxy of GOX, MOCVD has emerged as the most established technique for large-scale commercial growth. As far as the orientation of GOX is concerned, the principal planes, namely (100), (010), and (001) are often used for homoepitaxial thin-film growth. However, of these, only the (100) and (001) surface orientations are cleavage planes, making large diameter (> 6") wafer production possible. Despite the advantage offered by the (001) orientation, growth of high-quality MOCVD films on (001) GOX has not been reported. Here, we report the properties of GOX Schottky diodes on MOCVD-grown (001) films and compare the results to those grown on (010) substrates.

For this study, SBDs were fabricated on a Si-doped (001) 3.3-µm-thick homoepitaxial GOX thin film grown by MOCVD, where Ni was used as the Schottky metal. We also fabricated SBDs on a co-grown (010) film for comparison. The doping density in the films were in the range of 3-7 × 10^{15} cm^{-3} and 1.5-1.8 × 10^{16} cm^{-3} for the (001) and (010) samples, respectively, as determined by C-V measurements. From the room-temperature forward current density vs. voltage (J-V) characteristics, the ideality factor, Schottky barrier height (SBH), and on-resistance for (001) SBDs were extracted to be 1.07 eV, 1.08, and 25 mΩ-cm^2, respectively. The SBH for (001) was found to be ~ 0.17 eV lower than on (010). Further temperature-dependent analysis of the forward J-V characteristics show an apparent Schottky barrier inhomogeneity for the (001) samples. Reverse breakdown measurements showed an average breakdown voltage of 235 V, which is slightly lower than the value of 325 V predicted from TCAD. Poole-Frenkel analysis of the reverse J-V-T characteristics revealed excess leakage mechanism associated with the presence of traps at 0.31 eV below the conduction band which could also explain the early breakdown in the (001) layers. In summary, our study provides insights into the electrical characterization of SBDs fabricated on (001) GOX epitaxial films grown by MOCVD and highlights the need for optimizing growth parameters to improve film quality and device performance.

EP-TuP-8 Operation of β-Ga2O3 Field-effect Transistors at 650 °C, ***James Spencer Lundh,*** *H. Masten,* National Research Council Postdoctoral Fellow residing at US Naval Research Laboratory (DC)*; F. Alema, A. Osinsky,* Agnitron Technology, Inc.*; A. Jacobs, K. Hobart, T. Anderson, M. Tadjer,* US Naval Research Laboratory

The ultrawide bandgap of β-Ga2O3 (4.8 eV) allows high voltage/temperature operation, making it enticing for extreme environment electronics. Potential applications include space exploration, aeronautics, and defense, which can have operating environments with temperatures greater than 600°C. As such, performance and reliability at these high operating temperatures must be characterized and understood in order to optimize devices for expected, reliable, and stable operation. In this work, we report operation and electrical characterization of β-Ga2O3 metal-oxide-semiconductor field-effect transistors (MOSFETs) at temperatures up to 650°C to lay the groundwork for potential deployment in extreme environments.

Using Agnitron's Agilis 100 MOCVD reactor, a 300 nm thick UID Ga2O3 buffer, 30 nm thick 10^{18} cm^{-3} Ga2O3:Si channel, and 10 nm thick 10^{19} cm^{-3} Ga2O3:Si contact layers were grown on (010) β-Ga2O3:Fe substrates. Ti/Au Ohmic contacts were deposited (e-beam), lifted off, and annealed (470°C, 1 min, N2). Next, a 20 nm thick Al2O3 gate dielectric was deposited using ALD. Finally, Pt/Au gate contacts were deposited (e-beam). The devices had a channel width/length of 75/15.5 µm, gate length of 3 µm, and a drain-gate spacing of 10 µm. A cross-sectional schematic of the device structure is shown in Fig. 1. The MOSFETs had a Hall mobility of 170 $cm^2V^{-1}s^{-1}$, sheet carrier concentration of 1.74x10^{12} cm^{-2}, sheet resistance of 21.02 kΩ/sq, and specific contact resistivity of 5.26x10-4 Ωcm^2 at room temperature. For high temperature measurements, a DC/RF MicroXact probe station was used along with a Keithley 4200. All measurements were performed under vacuum at base temperatures (T_{base}) from 30°C to 654°C. The devices were held at T_{base}=654°C for 1 hr. DC output and transfer characteristics of a Ga2O3 MOSFET are shown in Fig. 2. From Fig. 2(a), at 654°C, there is >3× increase in the maximum Ids (Vgs = 5 V) as compared to at 30°C. In Fig. 2(b), a negative threshold voltage shift is observed as T_{base} is increased. Furthermore, the increase in T_{base} also led to a significant increase in the OFF-state leakage; from 30°C to 654°C, the leakage current increased by five orders of magnitude. In Fig. 3, both Ids and Ig are plotted as a function of Vgs for four MOSFETs at 654 °C. As shown, Ig is three orders of magnitude smaller than Ids in the OFF-state, indicating that the gate is not the primary leakage path at high temperatures. After returning to room temperature, the OFF-state leakage reduced to pre-heated levels and there was a slight improvement in the ON/OFF ratio.

Electronic and Photonic Devices, Circuits and Applications
Room Davis Hall 101 - Session EP+ET+MD-WeM

Process/Devices III
Moderator: Marko Tadjer, Naval Research Laboratory

10:45am **EP+ET+MD-WeM-10 Recent Progress of Ga_2O_3 Power Technology: Large-Area Devices, Packaging, and Applications***, Yuhao Zhang,* Virginia Tech **INVITED**

The Ga_2O_3 power device technology has witnessed fast advances towards power electronics applications. Recently, reports on large-area (ampere-class) Ga_2O_3 power devices have emerged globally, and their scope has gone well beyond the bare-die device demonstration into the device packaging, circuit testing, and ruggedness evaluation. These results have placed Ga_2O_3 in a unique position as the only ultra-wide bandgap semiconductor reaching these indispensable milestones for power device development. This talk will review the state of the art of the ampere-class Ga_2O_3 power devices (current up to >100 A and voltage up to >2000 V), covering the following topics:

1. Static electrical performance of Ga_2O_3 diodes and MOSFETs with ampere-class demonstrations (Fig. 1), with a summary of their key parameters including breakdown voltage, on-state current, and specific on-resistance (Fig. 2).
2. Dynamic performance of large-area Ga_2O_3 diodes and MOSFETs, including the reverse recovery, switching charge, as well as turn-ON and turn-OFF characteristics. A large-area Ga_2O_3 diode with NiO junction termination extension will be analyzed as a case study (Fig. 3).
3. Packaging and thermal management of Ga_2O_3 devices, highlighting the global efforts on junction-side packaging and cooling to overcome the low thermal conductivity of Ga_2O_3 (Fig. 4).
4. Circuit-level applications of Ga_2O_3 power devices, such as PFC circuits and double-pulse tests, as well as their circuit-level overcurrent/overvoltage ruggedness.

These results of large-area Ga_2O_3 devices allow for a direct comparison with commercial Si, SiC, and GaN devices. Accordingly, research opportunities and critical gaps for Ga_2O_3 power devices will also be discussed.

Reference:

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[2] Y. Qin *et al.*, "Thermal management and packaging of wide and ultra-wide bandgap power devices: a review and perspective," *J. Phys. Appl. Phys.*, vol. 56, no. 9, p. 093001, Feb. 2023.

[3] B. Wang *et al.*, "2.5 kV Vertical Ga2O3 Schottky Rectifier With Graded Junction Termination Extension," *IEEE Electron Device Lett.*, vol. 44, no. 2, pp. 221–224, Feb. 2023.

[4] B. Wang *et al.*, "Low Thermal Resistance (0.5 K/W) Ga_2O_3 Schottky Rectifiers With Double-Side Packaging," *IEEE Electron Device Lett.*, vol. 42, no. 8, pp. 1132–1135, Aug. 2021.

[5] M. Xiao *et al.*, "Packaged Ga2O3 Schottky Rectifiers With Over 60-A Surge Current Capability," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8565–8569, Aug. 2021.

11:15am **EP+ET+MD-WeM-12 Forward and Reverse Current Transport of (001) β-Ga_2O_3 Schottky Barrier Diodes and TiO_2/β-Ga_2O_3 Heterojunction Diodes with Various Schottky Metals***, Nolan Hendricks,* AFRL, UCSB*; E. Farzana,* UCSB*; A. Islam, D. Dryden, J. Williams,* Air Force Research Lab*; J. Speck,* UCSB*; A. Green,* Air Force Research Lab

β-Ga_2O_3 (BGO) has great potential for power devices due to its predicted breakdown field of 8 MV/cm, ease of n-type doping, and availability of melt-grown native substrates. The TiO_2/BGO heterojunction diode (HJD) has been shown to reduce reverse current compared to Schottky barrier diodes (SBDs) due to the high permittivity of TiO_2 without significantly affecting forward conduction losses due to the band alignment. [1] We demonstrate SBDs and HJDs with Ni, Pt, Cr, and Ti contacts, analyzing the current transport mechanism and showing similar or lower conduction losses in the HJD for all metals and reduced leakage current at higher electric fields in reverse bias.

SBDs and HJDs were fabricated on 8.5 µm of Si-doped BGO grown by HVPE on a Sn-doped (001) BGO substrate. Fabrication began with a backside Ti/Au cathode. 6.5 nm of TiO_2 was deposited on the HJD sample by plasma-enhanced ALD. Circular anode contacts (D=150 µm) of Pt/Au, Ni/Au, Cr/Au, and Ti/Au (20/180 nm) were patterned by separate lithography steps.

Capacitance-voltage (C-V) behavior was measured at 1 MHz. N_D-N_A and Φ_B were extracted from $1/C^2$. Current-voltage-temperature (J-V-T) characteristics of each device were measured, and Richardson plots were created from fitting the exponential region of each curve. Φ_B and the Richardson constant (A*) were extracted from each plot. Φ_B extracted for HJD is lower than in the SBD for Ni and Pt, while it is slightly higher for Cr. Unlike the Ti SBD, the Ti HJD showed rectifying behavior and exponential J-V in forward bias. Φ_B from C-V was similar but lower than J-V-T. In the linear-scale forward J-V characteristics at 25 °C, the lower Φ_B leads to lower V_{on}. No meaningful change in differential $R_{on,sp}$ is seen.

The reverse J-V behavior of each device at 25 °C was measured up to breakdown. To compare devices with different doping, J_R is plotted against the average electric field (E) at the BGO surface. In all cases, the HJDs saw higher E_{bk} than the corresponding SBDs. At lower field, the leakage current is higher in devices with lower Φ_B as expected from thermionic emission. However, at higher field, the leakage current is lower in all HJDs than the corresponding SBDs, indicating suppression of thermionic field emission current due to the wider energy barrier in the HJD. More detailed analysis indicating TFE as the primary leakage mechanism will be shown. Sharp increases in reverse current associated with defect-mediated soft breakdown are not observed for the HJDs. The reduced forward and reverse losses with higher V_{bk} of the TiO_2/BGO HJD demonstrate its potential to unlock the benefits of BGO in power diodes.

11:30am **EP+ET+MD-WeM-13 Vertical β-Ga_2O_3 Diodes with PtO_x/Interlayer Pt Schottky Contact and High Permittivity Dielectric Field Plate for Low Loss and High Breakdown Voltage***, Esmat Farzana, S. Roy, S. Krishnamoorthy, J. Speck,* University of California Santa Barbara

β-Ga_2O_3 is promising for high-power devices due to a bandgap of 4.8 eV, high breakdown field of 8 MV/cm, melt-grown substrates and shallow donors. However, the breakdown of β-Ga_2O_3 Schottky barrier diode (SBD) is often dictated by tunneling leakage through metal Schottky contacts with a limited Schottky barrier height (SBH) of 1.5 eV. Although oxidized noble metals (e.g, PtO_x) with SBH>2 eV can reduce tunneling leakage and improve breakdown voltage, the trade-off comes with increased on-state loss. Here, we report an alternative scheme of composite Schottky contact, PtO_x/Interlayer Pt, as a solution of reducing leakage but minimizing turn-on loss compared to PtO_x. As shown with vertical GaN SBDs,[1] the sputtered PtO_x with an interlayer e-beam deposited Pt, can reduce leakage, increase breakdown voltage, while enabling low turn-on voltage. Moreover, for edge leakage management, we integrated high permittivity ZrO_2 field-plate in these SBDs.

The SBDs were fabricated on halide vapor phase epitaxy (HVPE) (001) β-Ga_2O_3 of 10 µm epitaxy (doping ~1×10^{16} cm^{-3}). Three different Schottky contacts were fabricated, Pt, PtO_x (24 nm)/Interlayer Pt (1.5 nm), and PtO_x (24 nm). The PtO_x/Interlayer Pt SBDs were also investigated with a field-plate dielectric of 100 nm ZrO_2 (dielectric constant~26) on top of a 11 nm Al_2O_3 formed by atomic layer deposition (ALD) to protect the surface from sputtering-induced damage.

In bare SBDs, the forward current density-voltage (J-V) provided near unity ideality factor and SBHs of Pt (1.1 eV), PtO_x/Interlayer Pt (1.49 eV) and PtO_x (1.90 eV). The $1/C^2$-V provided similar trend of SBH with Pt (1.48 eV), PtO_x/Interlayer Pt (1.92 eV) and PtO_x (2.28 eV). Thus, the interlayer Pt allows tuning of SBH to lower values than PtO_x, leading to lower turn-on loss. All SBDs showed punchthrough breakdown where the fully depleted condition is reached at -910 V (estimated). The bare PtO_x/Interlayer Pt SBDs showed lower leakage and higher breakdown voltage (V_{br}) of 1.76 kV compared to Pt with 1.32 kV. The ZrO_2 field-plate further increased V_{br} to 2.34 kV. With a minimum on-resistance of 8 mΩ-cm^2, the Baliga's figure-of-merit (BFOM) of the field-plate SBD was obtained as 0.684 GW/cm^2. SILVACO simulation showed a parallel plane peak field of 3.25 MV/cm at anode center, peak field of 8 MV/cm at edge in β-Ga_2O_3, and 8.86 MV/cm in Al_2O_3. The barrier height engineering and field management involving processing techniques with reduced or minimal material damage presented

here is promising for realizing robust high performance β-Ga_2O_3 vertical power devices.

[1] Z. Shi et al., Semi. Sci. Tech. 37, 065010 (2022).

11:45am **EP+ET+MD-WeM-14 Ni/TiO_2/β-Ga_2O_3 Heterojunction Diodes with NiO Guard Ring Simultaneously Increasing Breakdown Voltage and Reducing Turn-on Voltage**, *J. Williams, N. Hendricks,* Air Force Research Lab*;* ***Weisong Wang,*** Wright State University*; A. Adams,* Apex Micro Devices*; J. Piel, D. Dryden, K. Liddy,* Air Force Research Lab*; N. Sepelak,* KBR Inc.*; B. Morell,* Cornell University*; A. Miesle,* University of Dayton*; A. Islam, A. Green,* Air Force Research Lab

β-Ga_2O_3 is an ultra-wide bandgap semiconductor (~4.8 eV) with numerous merits that potentially surpass the material limits other semiconductors for power electronic applications, namely a high predicted critical field strength of 8 MV/cm. Vertical Schottky barrier diodes (SBD) are a fundamental application for β-Ga_2O_3 to demonstrate power handling capabilities. However, breakdown behavior is limited by electric field crowding at the contact edge and high tunneling current under large reverse bias. We are reporting a novel integration of vertical heterojunction diode based on Ni/TiO_2/β-Ga_2O_3 with p-type NiO as the guard ring (GR). The heterojunction improves off-state losses and breakdown voltage (V_{bk}) without adding significant on-state losses. Leakage current is reduced by the additional barrier width, but the negative conduction-band offset between TiO_2 and β-Ga_2O_3 maintains low V_{on}. P-type NiO guard ring is to surround heterojunction to screen the high electric field generated at this region.

The devices were fabricated on an 8.5 µm Si-doped β-Ga_2O_3 drift region grown by HVPE on a heavily Sn doped (001) substrate. A back-side Ohmic contact was formed by evaporated Ti/Au. The NiO GR was created by sputtering and lift-off. A thin TiO_2 layer (42 Å) by ALD was shaped to overlap the anode. The Ni/Au anode was deposited before mesa was etched to provide edge termination to the SBD and HJD. The devices have circular contacts (D=100 µm) with an additional 5 µm GR. SBDs were co-fabricated on the same substrate as references. HJD showed a lower V_{on} (0.8 V) than the SBD (1.1 V) from linear extrapolation of the J-V curve. Temperature dependent I-V behavior was measured from 25 ºC to 200 ºC. Both device types show excellent fits to the thermionic emission model, and barrier heights of 0.6 eV and 1.2 eV were fit for the HJD and SBD respectively. The HJD had higher V_{bk} of 1190 V compared to the SBD (685 V), and the GR HJD saw even further improvement with V_{bk} of 1777 V (826 V for GR SBD). The BFOM ($V_{bk}^2/R_{on,sp}$) of 518 MW/cm^{2}for the GR HJD is competitive with other literature results.

This work demonstrates an average breakdown field beyond the material limits of SiC and GaN in a device that has even lower conduction losses than the co-fabricated SBD. Lowering V_{on} while raising V_{bk} simultaneously improves both on- and off-state parameters that are typically in competition with each other. With further optimized field management, the Ni/TiO_2/β-Ga_2O_3-HJD presents a path to realistically utilizing the high critical field of Ga_2O_3 without large forward conduction losses from a high-barrier junction.

12:00pm **EP+ET+MD-WeM-15 Fabrication of Self Aligned β-Ga_2O_3 Junction Barrier Schottky Diodes with NiO Field Termination**, ***Joseph Spencer,*** Naval Research Laboratory*; B. Wang, M. Xiao,* Virginia Tech*; A. Jacobs, T. Anderson, K. Hobart,* Naval Research Laboratory*; Y. Zhang,* Virginia Tech*; M. Tadjer,* Naval Research Laboratory

While the ultra-wide bandgap (4.8 eV) and the high critical field (6-8 MV/cm) of Ga_2O_3 is promising, the lack of shallow acceptors and the self-trapping of holes prevents this material from being doped p-type. The lack of complementary conductivity limits the practical device and termination structures for Ga_2O_3. Without the availability of p-type Ga_2O_3, Ga_2O_3 power devices must rely on a heterojunction for forming critically-important pn junctions. The naturally p-type nickel oxide (NiO, 3.6-4.5 eV [1]) forms a heterojunction with Ga_2O_3 and has been used to demonstrate Ga_2O_3 JBS diodes [2, 3].

In this work we have developed a self-aligned JBS diode fabrication process at 1 µm resolution that is capable of withstanding high-temperature thermal and chemical treatments such as annealing and relevant plasma/acid etches for Ga_2O_3 (e.g., BCl_3, HCl, H_3PO_4). This novel dry lift-off process incorporates a XeF_2 etch for undercut and lift-off steps producing a self-aligned process enabling fine device features without misalignment. A tri-layer mask consisting of, in order of deposition, amorphous Silicon (a-Si), SiO_2, and Ni, allow for the dry etching of the Ga_2O_3 epilayer prior to NiO self-aligned deposition. The Ni, SiO_2, and a-Si layers were patterned using Transene Ni-etchant, CF_4-plasma, and a SF_6-plasma dry etching, respectively. Subsequently, a ~250 nm deep trench in the Ga_2O_3 epilayer was etched via BCl_3 plasma, and a post-dry etch clean in warm (80 °C) H_3PO_4 was performed for 10 minutes, wherein the Ni hard mask was also removed. The a-Si mask layer was undercut using a 1" burst of dilute XeF_2 in a Xactix XeF_2 etcher. P-type NiO with 10% O_2 was sputtered (200 W, 12.5 mTorr) in the trench regions, followed by a dry lift-off of the remaining mask (a-Si/SiO_2) in XeF_2 gas by selective undercutting of the a-Si layer. At the conclusion of this self-aligned process, a tri-layer NiO junction termination extension (JTE) region was deposited around the anode perimeter in order to facilitate electric field spreading and improve V_{BR} [4]. Ni/Au anode was deposited atop the JBS region and the inner portions of the NiO JTE to conclude device fabrication (Figs. 1-4). Current-voltage characteristics in forward and reverse bias are shown in Figs. 5-6, respectively. This novel self-aligned process as shown by the fabrication of Ga_2O_3 NiOJBS diode serves to advance Ga_2O_3 heterojunction device technology and fabrication capabilities.

12:15pm **EP+ET+MD-WeM-16 Ni/$BaTiO_3$/β-Ga2O3 Solar-Blind UV Photodetectors with Deep Etch Edge Termination**, ***Nathan Wriedt,*** *S. Rajan,* Ohio State University

We report on the design and demonstration Ni/$BaTiO_3$/β-Ga_2O_3 photodetectors, where high-permittivity $BaTiO_3$ is introduced to enable high fields approaching the material (avalanche breakdown) limit. β-Ga_2O_3 has a bandgap of 4.8eV and a corresponding photon absorption edge at 270-280nm, making it a prime candidate for utilization in solar blind UV photodetectors applications. Furthermore, the excellent material quality and low doping densities achievable through epitaxy on bulk-grown substrates can enable extremely low dark currents. Schottky diodes suffer breakdown well before the 8 MV/cm material limit. However, inserting the extreme-k $BaTiO_3$ dielectric between the metal and β-Ga_2O_3 prevents tunneling breakdown of the metal-semiconductor interface, and has been shown to support extremely high breakdown fields in β-Ga_2O_3 [1].When high electric fields occur in the β-Ga_2O_3 the electric field in the $BaTiO_3$ is low due to the relative permittivity, thus maintaining a tunneling barrier. Additionally, the valence band offset between the $BaTiO_3$ and Ga_2O_3 presents no barrier to transport of holes. Device were fabricated using (001)-oriented HVPE-grown Ga_2O_3 films (10-µm, N_d=1x10^{16} cm^{-3}) on Sn-doped Ga_2O_3 bulk substrates. The device structure investigated consisted of 1000 µm diameter circular mesas where the epitaxial layer was etched using a BCl_3/Cl_2-based ICP-RIE process to produce 0, 3, and 6-um pillars that have been shown to be effective in achieving high junction termination efficiency [2]. 10 nm $BaTiO_3$ was then deposited conformally by RF sputtering onto the etched surface. Device fabrication was completed by e-beam evaporation of Ti/Au backside ohmic contact and Ni top contacts. Extremely low dark currents (~0.25nA/cm^2) were measured under reverse bias up to 200 V. The devices showed an excellent UV/visible rejection ratio [R(244)/R(400)=3.65 *10^7]. We estimated the peak responsivity to be 970 mA/W at 244 nm at a reverse bias of -20 V. In conclusion, the work here shows the promise of Ni/$BaTiO_3$/β-Ga_2O_3 for realizing photodetectors with excellent operating characteristics. This work lays the foundation for future studies where the high breakdown strength enabled by $BaTiO_3$ could enable the design of solar-blind photodetectors with avalanche gain. We acknowledge funding from Department of Energy / National Nuclear Security Administration under Award Number(s) DE-NA0003921, and AFOSR GAME MURI (Award No. FA9550-18-1-0479, project manager Dr. Ali Sayir).[1] Xia et al, Appl. Phys. Lett. 115, 252104 (2019)[2]Dhara et al, Appl. Phys. Lett. 121, 203501 (2022)

12:30pm **EP+ET+MD-WeM-17 Best Paper Awards, e-Surveys, and Closing Remarks**,

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