Two-Dimensional Analytical Modeling of the Surface Potential of a Double-Gate Vertical Fin-Shaped Ga_2O_3 Power Transistor

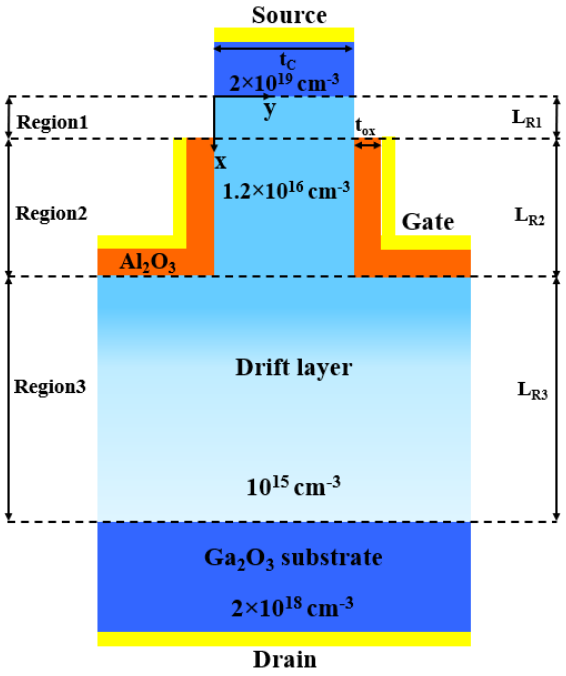

Fig 1: Vertical Ga_2O_3 Device structure used for analytical modeling. The entire unit is divided into three region. The lengths of the depletion region that are created in the source–channel and channel–drain junctions are denoted by L_{R1} and L_{R2}, respectively. The drift layer length is denoted as L_{R3}. The junctions between the source-channel and drain-channel are intended to be abrupt for the sake of simulation.

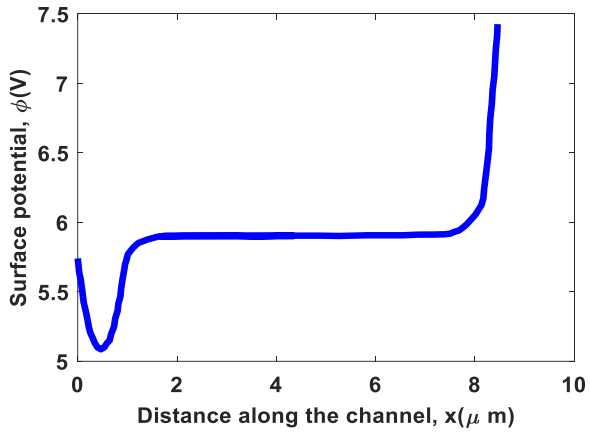

Fig 2: Surface potential of vertical Ga_2O_3 PowerFET. The potential is increased in parabolic manner at the source-channel and channel-drain junction.

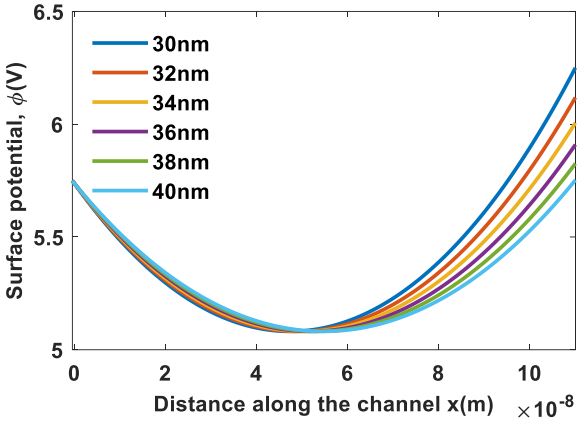

Fig 3: Surface potential profile along the channel with varying oxide thickness. The potential is decreasing as the oxide thickness (t_{ox}) increases, which causes the gate to eventually lose control of the channel.

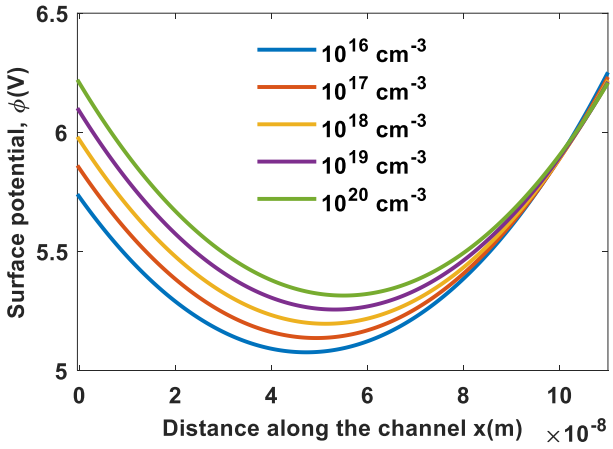

Fig 4. Surface potential profile along the channel for varying doping concentration. The potential on the source-channel junction increases for the same gate-source voltage as the accumulation of charge carrier beneath the channel rises.