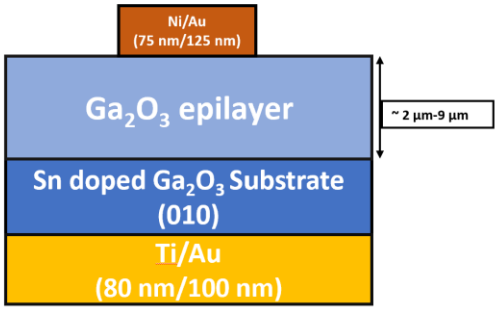

Table I. Growth conditions of β-Ga_2O_3 films on the Sn-doped β-Ga_2O_3 substrate

Sample No	Epilayer Thickness (µm)	Estimated Growth Rate	Target Doping (cm^{-3})
S1	9.5	3 µm/hr	2-3 × 10^{16}
S2	3	650 nm/hr	2 × 10^{16}
S3	2	650 nm/hr	7 × 10^{16}

Fig. 1. Schematic cross-section of the vertical Schottky diode structures

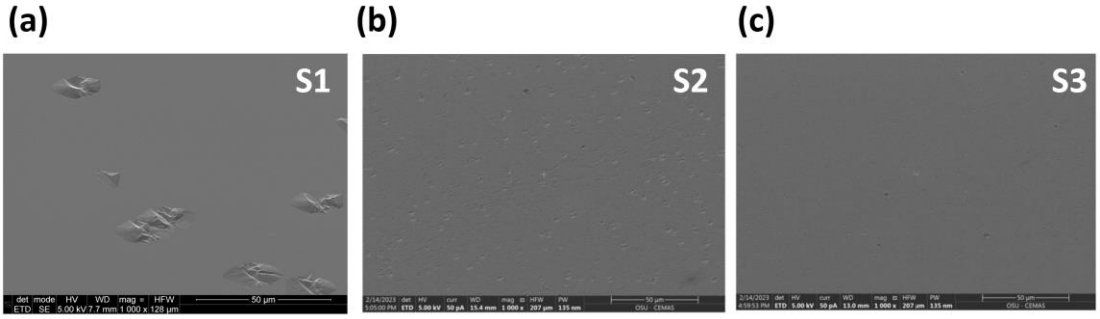

Fig. 2. FESEM images of MOCVD grown β-Ga_2O_3 films on Sn-doped β-Ga_2O_3 substrates for all the Schottky diodes associated with this study. The figure below also shows that S3 has the smoothest surface than the other two samples.

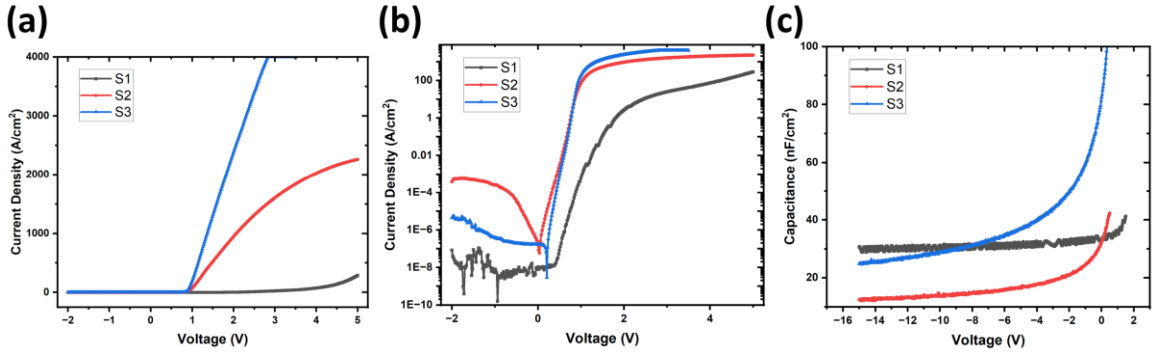

Fig. 3. (a) Room temperature current density (*J*) vs. voltage (*V*) characteristics for S1, S2, and S3 Schottky barrier diodes. (b) Semi-logarithmic *J-V* characteristics for S1, S2, and S3 Schottky barrier diodes. (c) Room temperature reverse bias capacitance (C)-voltage (V) data for S1, S2, and S3 Schottky barrier diodes.

Table II. Extracted electrical properties at room temperature for S1, S2, and S3.

Sample No	Ideality Factor	Barrier Height (eV)	$R_{on,sp}$ (mΩ.cm^2)	ON-OFF Ratio	Average Doping (cm^{-3})
S1	2.17	1.42	17.36	$>10^9$	2.02 × 10^{16}
S2	1.73	1.18	1.87	$>10^7$	1.73 × 10^{16}
S3	1.31	1.0	0.707	$>10^8$	6.08 × 10^{16}