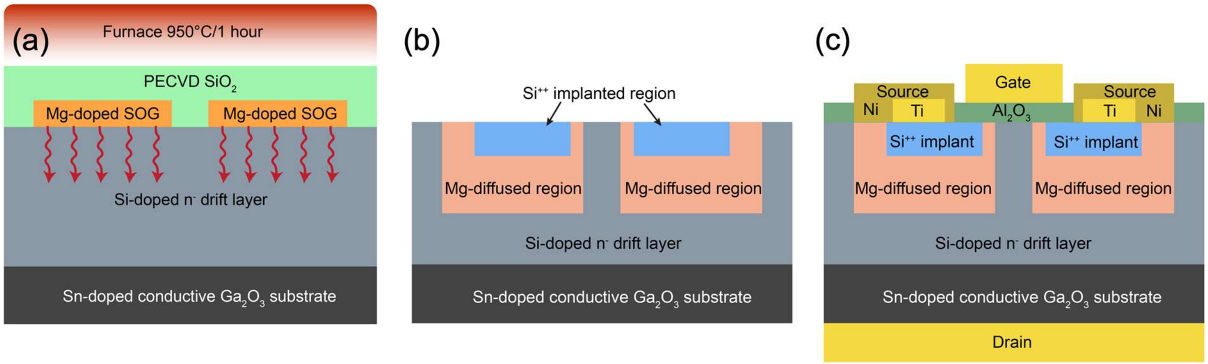

Fig. 1. Fabrication process flow of the β-Ga_2O_3 VDBFET. (a) shows the patterned Mg-SOG diffusion doping process; (b) shows the schematic after the source Si^+ ion implantation; (c) shows the cross-section schematic of the final fabricated device.

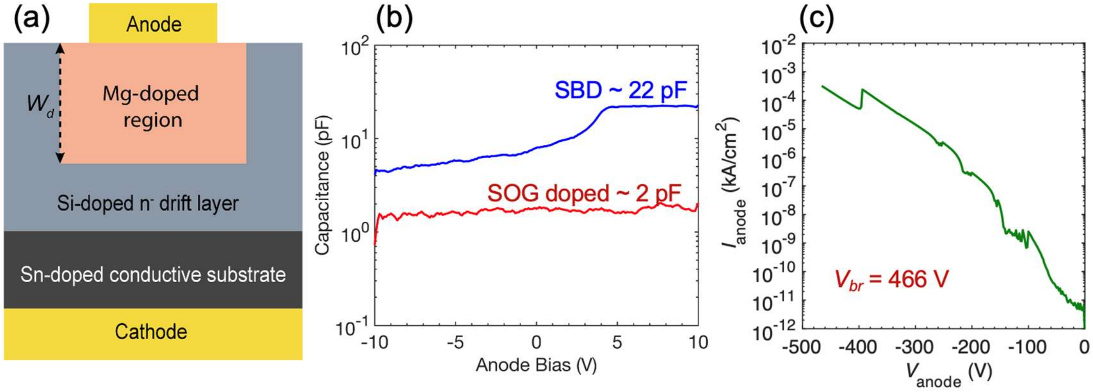

Fig. 2. (a) The metal-isolation-semiconductor (MIS) test structure used for CV analysis shown in (b) and the IV analysis shown in (c).

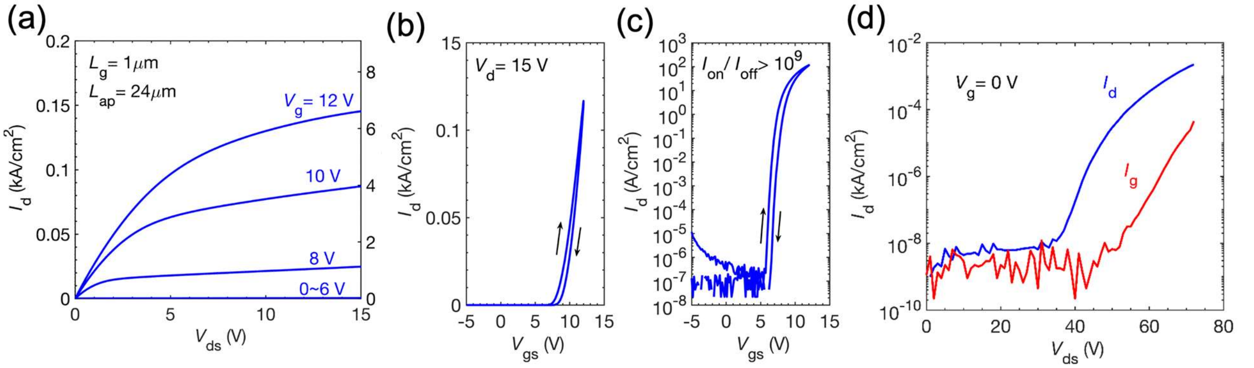

Fig. 3. Representative (a) output IV characteristic, transfer characteristic in (b) linear, (c) log scale and the breakdown characteristic of the fabricated Ga_2O_3 VDBFET.