Electronic and Photonic Devices, Circuits and Applications Room Bansal Atrium - Session EP-TuP

Electronic and Photonic Devices, Circuits and Applications Poster Session II

EP-TuP-6 Investigating the Properties of β-Ga_2O_3 Schottky Diodes on MOCVD-Grown (001) Drift Layer, ***Prakash P. Sundaram,*** University of Minnesota, USA*; F. Alema, A. Osinsky,* Agnitron Technology*; S. Koester,* University of Minnesota, USA

In this study, we investigate the electrical properties of Schottky barrier diodes (SBD) fabricated on epitaxial layers grown on (001) β-Ga_2O_3 (GOX) by metal-organic chemical vapor deposition (MOCVD). While various growth methods have been used for epitaxy of GOX, MOCVD has emerged as the most established technique for large-scale commercial growth. As far as the orientation of GOX is concerned, the principal planes, namely (100), (010), and (001) are often used for homoepitaxial thin-film growth. However, of these, only the (100) and (001) surface orientations are cleavage planes, making large diameter (> 6") wafer production possible. Despite the advantage offered by the (001) orientation, growth of high-quality MOCVD films on (001) GOX has not been reported. Here, we report the properties of GOX Schottky diodes on MOCVD-grown (001) films and compare the results to those grown on (010) substrates.

For this study, SBDs were fabricated on a Si-doped (001) 3.3-µm-thick homoepitaxial GOX thin film grown by MOCVD, where Ni was used as the Schottky metal. We also fabricated SBDs on a co-grown (010) film for comparison. The doping density in the films were in the range of 3-7 × 10^{15} cm^{-3} and 1.5-1.8 × 10^{16} cm^{-3} for the (001) and (010) samples, respectively, as determined by C-V measurements. From the room-temperature forward current density vs. voltage (J-V) characteristics, the ideality factor, Schottky barrier height (SBH), and on-resistance for (001) SBDs were extracted to be 1.07 eV, 1.08, and 25 mΩ-cm^2, respectively. The SBH for (001) was found to be ~ 0.17 eV lower than on (010). Further temperature-dependent analysis of the forward J-V characteristics show an apparent Schottky barrier inhomogeneity for the (001) samples. Reverse breakdown measurements showed an average breakdown voltage of 235 V, which is slightly lower than the value of 325 V predicted from TCAD. Poole-Frenkel analysis of the reverse J-V-T characteristics revealed excess leakage mechanism associated with the presence of traps at 0.31 eV below the conduction band which could also explain the early breakdown in the (001) layers. In summary, our study provides insights into the electrical characterization of SBDs fabricated on (001) GOX epitaxial films grown by MOCVD and highlights the need for optimizing growth parameters to improve film quality and device performance.

EP-TuP-8 Operation of β-Ga2O3 Field-effect Transistors at 650 °C, ***James Spencer Lundh,*** *H. Masten,* National Research Council Postdoctoral Fellow residing at US Naval Research Laboratory (DC)*; F. Alema, A. Osinsky,* Agnitron Technology, Inc.*; A. Jacobs, K. Hobart, T. Anderson, M. Tadjer,* US Naval Research Laboratory

The ultrawide bandgap of β-Ga2O3 (4.8 eV) allows high voltage/temperature operation, making it enticing for extreme environment electronics. Potential applications include space exploration, aeronautics, and defense, which can have operating environments with temperatures greater than 600°C. As such, performance and reliability at these high operating temperatures must be characterized and understood in order to optimize devices for expected, reliable, and stable operation. In this work, we report operation and electrical characterization of β-Ga2O3 metal-oxide-semiconductor field-effect transistors (MOSFETs) at temperatures up to 650°C to lay the groundwork for potential deployment in extreme environments.

Using Agnitron's Agilis 100 MOCVD reactor, a 300 nm thick UID Ga2O3 buffer, 30 nm thick 10^{18} cm^{-3} Ga2O3:Si channel, and 10 nm thick 10^{19} cm^{-3} Ga2O3:Si contact layers were grown on (010) β-Ga2O3:Fe substrates. Ti/Au Ohmic contacts were deposited (e-beam), lifted off, and annealed (470°C, 1 min, N2). Next, a 20 nm thick Al2O3 gate dielectric was deposited using ALD. Finally, Pt/Au gate contacts were deposited (e-beam). The devices had a channel width/length of 75/15.5 µm, gate length of 3 µm, and a drain-gate spacing of 10 µm. A cross-sectional schematic of the device structure is shown in Fig. 1. The MOSFETs had a Hall mobility of 170 $cm^2V^{-1}s^{-1}$, sheet carrier concentration of 1.74x10^{12} cm^{-2}, sheet resistance of 21.02 kΩ/sq, and specific contact resistivity of 5.26x10-4 Ωcm^2 at room temperature. For high temperature measurements, a DC/RF MicroXact probe station was used along with a Keithley 4200. All measurements were performed under vacuum at base temperatures (T_{base}) from 30°C to 654°C. The devices were held at T_{base}=654°C for 1 hr. DC output and transfer characteristics of a Ga2O3 MOSFET are shown in Fig. 2. From Fig. 2(a), at 654°C, there is >3× increase in the maximum Ids (Vgs = 5 V) as compared to at 30°C. In Fig. 2(b), a negative threshold voltage shift is observed as T_{base} is increased. Furthermore, the increase in T_{base} also led to a significant increase in the OFF-state leakage; from 30°C to 654°C, the leakage current increased by five orders of magnitude. In Fig. 3, both Ids and Ig are plotted as a function of Vgs for four MOSFETs at 654 °C. As shown, Ig is three orders of magnitude smaller than Ids in the OFF-state, indicating that the gate is not the primary leakage path at high temperatures. After returning to room temperature, the OFF-state leakage reduced to pre-heated levels and there was a slight improvement in the ON/OFF ratio.

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