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Electronic and Photonic Devices, Circuits and Applications
Room Jefferson 1 & Atrium - Session EP-MoP

Electronic and Photonic Devices, Circuits and Applications
Poster Session

EP-MoP-2 Gate Effects of Channel and Sheet Resistance in β-Ga_2O_3 Field-Effect Transistors using the TLM Method, ***Ory Maimon***, Department of Electrical Engineering, George Mason University; *N. Moser,* Air Force Research Laboratory, Sensors Directorate; *K. Liddy, A. Green, K. Chabak,* Air Force Research Laboratory, Sensors Directorate, USA; *C. Richter, K. Cheung, S. Pookpanratana,* Nanoscale Device and Characterization Division, National Institute of Standards and Technology; *Q. Li,* Department of Electrical Engineering, George Mason University

Beta Gallium Oxide (β-Ga_2O_3) is a rapidly developing semiconductor for high power electronic devices with promising advantages. Accurate characterization of the resistances in β-Ga_2O_3 field-effect transistors (FET) are critical to understand and model these devices. Here, we report on extracting contact, channel, and sheet resistances from planar, depletion-mode β-Ga_2O_3 FETs using the transfer length method (TLM). The results are analyzed in comparison with conventional TLM structures fabricated on the same wafer. The β-Ga_2O_3 FETs are composed of a 50-nm Si-doped epi-layer with a target concentration of 2.4 x 10^{18} cm^{-3} fabricated on a (010) semi-insulating β-Ga_2O_3 substrate. Aluminum oxide (Al_2O_3, 20 nm) was used as the gate dielectric and the gate length (L_G) remained constant at 1.94 µm, while the source-drain spacing (L_{SD}) varied as 3µm, 8 µm, and 13 µm. No back contact was used due to the semi-insulating substrate. Transfer characteristic measurements were taken at room temperature and low drain-source voltage (V_{DS}) of 0.01 V to suppress drain effects on the threshold voltage (V_{TH}), about -4 V, for devices at different L_{SD} spacing.

When compared to the TLM structures, we observe a decrease in extracted sheet resistance (R_{sh}), and channel sheet resistance (R_{ch}) as the channel turns on with increasing gate-source voltage (V_{GS}). The contact resistance (R_C) is assumed to be constant, and is found to be 27.7 Ω mm at a V_{GS} of 0 V. From a V_{GS} of -3 V to 3 V (off to on state), R_{sh} quickly decreases from 90.4 kΩ sq^{-1} and appears to plateau at 28.2 kΩ sq^{-1}. We saw a similar trend for R_{ch}, which decreased from 288 kΩ sq^{-1} to 7.66 kΩ sq^{-1}. From the channel sheet resistance, we can find an accurate field-effect mobility after removing the parasitic resistances. A FET with an L_{SD} of 3µm was found to have a field-effect mobility of 61 cm^2 V^{-1} s^{-1} at a V_{GS} of 3 V. This work indicates that the channel resistance can be accurately extracted by applying the TLM method to FETs, and further helps understand β-Ga_2O_3 gate effects on transistor performance.

EP-MoP-3 Lateral β-Ga_2O_3 Schottky Barrier Diodes With Interdigitated Contacts, ***Jeremiah Williams***, Air Force Research Laboratory, Sensors Directorate; *A. Arias-Purdue,* Teledyne; *K. Liddy, A. Green,* Air Force Research Laboratory, Sensors Directorate; *D. Dryden, N. Sepelak,* KBR; *K. Singh,* Air Force Research Laboratory, Sensors Directorate; *F. Alema, A. Osinsky,* Agnitron Technology; *A. Islam, N. Moser, K. Chabak,* Air Force Research Laboratory, Sensors Directorate

This work characterizes a lateral β-Ga_2O_3 Schottky barrier diode (SBD) with an interdigitated contact design fabricated using a homoepitaxial thin-film. This SBD design can be monolithically integrated into RF power switching circuits with standard lateral FET processing. This technique avoids complex fabrication and losses from heterogeneous integration while maintaining the fast switching capabilities of a thin, lateral channel. Prior literature has shown impressive performance from vertical SBDs [1] and lateral devices on non-native substrates [2], but lateral SBDs on homoepitaxial β-Ga_2O_3 thin-films are not well explored. To the authors' knowledge, this is the first demonstration of such a SBD design in β-Ga_2O_3.

The β-Ga_2O_3 epitaxial layer is grown by MOCVD with a target thickness of 65 nm. Hall effect measurements indicate Si doping of 3.347e17 cm^{-3}, carrier mobility of 86.5 cm^2/V-s, and a sheet resistance of 33.15 kΩ/sq. A surface RMS roughness of 0.839 nm is measured by AFM. Mesa isolation is achieved with a BCl_3 ICP etch. Ohmic contacts are formed by Si ion implantation and a metal stack of Ti/Al/Ni/Au (25/120/50/50 nm) annealed at 470°C. Implant carrier concentration is measured at 5.976×10^{19} cm^{-3}. Evaporated Pt/Au (20/380 nm) forms the Schottky contact. The first passivation layer is 30 nm of Al_2O_3 deposited by ALD patterned with BOE. Next, a metal interconnect layer of Ir/Au (10/380 nm) is deposited. Final passivation is ~85 nm of Al_2O_3 by ALD pattered with a CF_4 RIE etch. All metal is pattered by photoresist lift off.

The diode features four 4x50 µm anode fingers interdigitated with five 8x50 µm cathode fingers. The anode-cathode spacing is 5 µm. The Pt-Ga_2O_3 barrier height is extracted from temperature dependent J-V measurements to be 1.742 eV. Fitting to forward bias J-V measurements shows an ideality factor of 2.246 and a build-in voltage of 1.963 V. The diode has a breakdown voltage (V_{bk}) of 784 V and a specific on-resistance ($R_{on,sp}$) of 9.133 Ω-cm^2, normalized to the current carrying region between contacts. This yields a power figure of merit (PFOM) of 67.3 MW/cm^2. We attribute the poor ideality to the highly resistive epitaxy and the degraded interface caused by the relatively rough surface. This device is competitive with published lateral SBD results, and establishes a baseline to enable further development of β-Ga_2O_3 RF power switching circuits with a streamlined, monolithic fabrication process.

[1] S. Roy *el al.*, *IEEE Electron Device Lett.*, **34**, 8, (2021).

[2] Z. Hu *et al.*, *IEEE Electron Device Lett.*, **39**, 10, (2018).

EP-MoP-4 Optimized Annealing for Activation of Implanted Si in β-Ga2O3, ***Katie Gann***, *J. McCandless,* Cornell University; *T. Asel, S. Tetlak,* Air Force Research Laboratory; *D. Jena, M. Thompson,* Cornell University

Ion implantation of β-Ga_2O_3 will be critical for low resistance contacts and advanced device structures. Literature suggests good activation of Si implants after annealing under N_2, but reversible deactivation of carriers under O_2-rich annealing. However, there have been no significant studies establishing annealing behavior as a function of time, temperature, and controlled gas ambients. Unintentionally doped (UID) β-Ga_2O_3 films, grown by plasma assisted molecular beam epitaxy on Fe-doped semi-insulating β-Ga_2O_3 substrates with a UID thickness >400 nm, were ion implanted with Si to a total dose of 7x10^{14} cm^{-2} at three energies (15-115 keV) through an SiO_2 cap (20 nm) to yield a 100 nm box profile with a concentration of 5x10^{19} cm^{-3}. Secondary ion mass spectrometry (SIMS) was used to compare implant profiles to SRIM simulated ion ranges, and to quantify Si diffusion during annealing. A wide range of annealing conditions were studied using a load-locked ultrahigh vacuum compatible quartz tube furnace with precise gas control. Anneal times were varied from 10 to 120 minutes, temperatures from 850 to 1000 °C, and the anneal ambient gas was varied by mixing research plus (RP) N_2 with ultra-high purity (UHP) O_2 to control the oxygen partial pressure (pO_2) between <10^{-6} and 1.0 bar. Gases were also selectively passed over a desiccant to reduce the water vapor partial pressure to <10^{-8} bar. Sheet resistance, carrier activation, and mobility were determined using van der Pauw structures. Annealing in extremely low pO_2 (forming gas 4% H_2/N_2) resulted in decomposition of the Ga_2O_3, while annealing at pO_2 above 10^{-2} bar resulted in minimal carrier activation. Within the moderate pO_2 range, minimizing the partial pressure of water vapor was shown to be critical to achieve high carrier activation, with the negative impact of water vapor becoming more significant with increasing pO_2. Data, however, suggests that a trace level of water vapor may slightly improve carrier activation.Short duration anneals resulted in higher carrier activation with longer times resulting in "over annealing" and reduced carrier density. Optimal anneal temperatures were determined to be between 900 and 950 °C, with lower temperatures showing reduced mobility and higher temperatures exhibiting reduced carrier activation and increased Si diffusion. The optimized anneal conditions for this implant were found to be at 950 °C for 20 minutes under dried RP N_2, with an extended gas purge of the furnace prior to the anneal to remove any residual water vapor, resulting in 88% carrier activation and a mobility of 72 cm^2/V-s (R_s = 130 Ω/sq).

Electronic and Photonic Devices, Circuits and Applications
Room Jefferson 2-3 - Session EP1-WeM

Process & Devices III

Moderator: Uttam Singisetti, University of Buffalo, SUNY

9:15am **EP1-WeM-4 Remarkable Improvement of Conductivity in B-Ga_2O_3 by High-Temperature Si Ion Implantation**, ***Arka Sardar***, *T. Isaacs-Smith, S. Dhar,* Auburn University*; J. Lawson, N. Merrett,* Air Force Research Laboratory, USA

Monoclinic Beta Gallium Oxide (β-Ga_2O_3) is emerging as a promising wide bandgap semiconductor for high voltage electronics. Ion implantation is a key process for device fabrication as it provides a unique way to carry out selective area doping with excellent control. It has been demonstrated that Si implantation into (010) β-Ga_2O_3 at room temperature followed by annealing at ~1000°C, results in an activation efficiency (η)of 63% for Si concentrations up to ~5e19 cm^{-3}. However, for higher concentrations, a severe drop of the η to 6% occurs [1]. In this work, we demonstrate that high-temperature implantation can be used to significantly improve this for heavily implanted β-Ga_2O_3. In the case of SiC, implantation at > 500°C results in superior conductivity due to lower defect densities and better recrystallization after annealing [2]. Based on this, we performed room temperature (RT, 25°C) and high temperature (HT, 600°C) Si implants into MBE grown 300 nm (010) β-Ga_2O_3 films with energies of 275 keV and 425 keV through ~110 nm Mo and ~30 nm Al_2O_3 layers; with a total of fluence of 2.4e15 cm^{-2} or 4.8e15 cm^{-2}. This was followed by annealing in flowing nitrogen at 970°C for 30 minutes to activate the dopants. SIMS shows the Si profile is ~400 nm deep with an average concentration of ~6.0e19 cm^{-3} for the lower fluence samples, and expected to be ~1.2e20cm^{-3} for the higher fluence (SIMS ongoing). No significant difference in surface roughnesses were detected by AFM throughout the process. HRXRD shows structural defects after the implantation and partial crystallization recovery upon annealing, where the advantage was in favor of HT implantation. The ratio of the free electron concentration from Hall measurements and the total amount of Si in β-Ga_2O_3 was used to determine the activation efficiencies. For the lower fluence, the HT sample shows only a ~6% improvement of η over the RT sample. Remarkably, for the higher fluence, while the RT sample was too resistive for measurement, the HT sample had η close to 70%, with a high sheet electron concentration of 3.3e15 cm^{-2} and excellent mobility of 92.8 $cm^2/V{\cdot}s$ at room temperature. These results are highly encouraging for achieving ultra-low resistance heavily doped β-Ga_2O_3 layers using ion implantation, which will be discussed further in this presentation.

References:

[1]K. Sasaki et.al,, Appl. Phys. Express 6, 086502 (2013).

[2]F. Roccaforte, et. al, , Micro 2, 23 (2022).

Acknowledgments:

We acknowledge the support of the Department of Physics, Auburn University.

9:30am **EP1-WeM-5 Towards Lateral and Vertical Ga_2O_3 Transistors for High Voltage Power Switching**, ***Kornelius Tetzner***, *J. Würfl, E. Bahat-Treidel, O. Hilt,* Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik (FBH), Germany*; Z. Galazka, S. Bin Anooz, A. Popp,* Leibniz-Institut für Kristallzüchtung (IKZ), Germany **INVITED**

Gallium Oxide (Ga_2O_3) power switching devices are expected to boost efficiency of power converters predominately operating at comparatively high bias voltage levels in the kV range. Thanks to the extraordinarily high energy band gap of 4.9 eV a high device breakdown strength of about 8 MV/cm is expected. Thus it is possible to efficiently utilize these properties for very compact power devices with aggressively minimized gate to drain separation. This enables low resistive on-state and low leakage off-state properties. Most Ga_2O_3 devices introduced so far rely on volume electron transport properties; only a few 2DEG devices have been demonstrated. In any case the values of electron mobility and saturation velocity in Ga_2O_3 crystals may depend on crystal orientation and did not yet reach properties being comparable to more developed wide band gap semiconductor families such as GaN and SiC. – Nevertheless the benefit of Ga_2O_3 devices relates to the combination of high breakdown field and electron transport properties and the resulting compact device design strategies are already getting competitive to existing power switching technologies.

The presentation will give an overview on the current status of lateral and vertical Ga_2O_3 devices with a special emphasis on results obtained at FBH and IKZ [1]. For both cases concepts for epitaxial layer structures and device designs suitable for reaching the targeted performance will be discussed especially in terms of breakdown voltage and channel current density. Critical points for device optimization such as type of gate recess in lateral transistors and concepts of critical electric field reduction in vertical transistors will be addressed.

[1] K. Tetzner, IEEE Electron Device letters, vol. 40, No. 9, (2019), pp. 1503 - 1506.

10:00am **EP1-WeM-7 Comparison of β-Ga_2O_3 Mosfets With TiW and NiAu Metal Gates for High-Temperature Operation**, ***Nicholas Sepelak***, KBR, Wright State University*; D. Dryden,* KBR*; R. Kahler,* University of Texas at Dallas*; J. William,* Air Force Research Lab, Sensors Directorate*; T. Asel,* Air Force Research Laboratory, Materials and Manufacturing Directorate*; H. Lee,* University of Illinois at Urbana-Champaign*; K. Gann,* Cornell University*; A. Popp,* Leibniz-Institut für Kristallzüchtung, Germany*; K. Liddy,* Air Force Research Lab, Sensors Directorate*; K. Leedy,* Air Force Research Laboratory, Sensors Directorate*; W. Wang,* Wright State University*; W. Zhu,* University of Illinois at Urbana-Champaign*; M. Thompson,* Cornell University*; S. Mou,* Air Force Research Laboratory, Materials and Manufacturing Directorate, USA*; K. Chabak, A. Green,* Air Force Research Laboratory, Sensors Directorate*; A. Islam,* Air Force Research Laboratory, Sensors Directory

β-Ga_2O_3 offers a robust platform for operation of electronic devices at a high temperature because of its large band gap and low intrinsic carrier concentration. We have recently characterized the high temperature performance β-Ga_2O_3 field effect transistors using different gate metals in vacuum and air ambient at temperatures up to 500 °C.

The devices fabricated using TiW refractory metal gate and Al_2O_3 gate dielectric exhibited stable operation up to 500 °C in vacuum and up to 450 °C in air [1]. Transfer (I_{DS}-V_{GS}) characteristics of a device were measured at various temperatures in vacuum and air. Extracted I_{MAX}/I_{MIN} for the vacuum test reduced from ~10^4 to 10^2 as temperature was increased up to 500 °C. During the vacuum characterization, the contact resistance remained unchanged at all temperatures and, therefore, device characteristics showed no degradation once devices were brought back to RT even after several hours of device operation at 500 °C in vacuum.

The devices, fabricated with Ni/Au gate metal and Al_2O_3 gate dielectric, exhibited stable operation up to 500 °C in air [2]. The measured I_D-V_D characteristics showed no current degradation up to 450 °C. At 500 °C, the device exhibited a drop in I_D; however, device characteristics recovered once the device is brought back to RT, even after 20 hours of device operation at 500 °C.

For tests in air ambient, both Ni/Au and Ti/W devicesobserved an increase in current with temperature due to activation carriers from dopants/traps in the device, however, both exhibited $I_{MAX}/I_{MIN} < 10^2$ at 450 °C because of contact degradation. The barrier height of ϕ_B~ 1.0 eV and 0.77 eV was calculated for the TiW/Al_2O_3 and the NiAu/Al_2O_3 interfaces, respectively using thermionic emission theory. Thought the values of ϕ_B for the Ti/W contacts was consistent with that expected from the work-function difference between TiW and Al_2O_3, the devices with Ni/Au yielded lower ϕ_B presumably due to the diffusion of Ni and the partial crystallization of the Al_2O_3 dielectric [3]. Our results suggest that with appropriate choice of metals and gate dielectrics, the stable 500 °C operation using β-Ga_2O_3 is achievable.

[1] Sepelak *et al*., "High-temperature operation of β-Ga_2O_3 MOSFET with TiW refractory metal gate," *DRC, 2022*.

[2] Sepelak *et al*., "First Demonstration of 500 °C Operation of β-Ga_2O_3 MOSFET in Air," *CSW, 2022*

[3] Islam et al., "Thermal stability of ALD-grown SiO2 and Al2O3 on (010) β-Ga2O3 substrates," DRC, 2022.

10:15am **EP1-WeM-8 High Electron Mobility Si-doped β-Ga_2O_3 MESFETs**, ***Arkka Bhattacharyya***, University of Utah*; S. Roy,* University of California at Santa Barbara*; P. Ranga,* University of Utah*; S. Krishnamoorthy,* University of California at Santa Barbara

A hybrid low temperature - high temperature (LT-HT) buffer/channel stack growth is demonstrated using MOVPE with superior carrier mobility values. An LT-grown (600°C) undoped Ga_2O_3 buffer (250-330 nm thick) is grown

followed by transition layers to a HT (810°C) Si-doped Ga_2O_3 channel layers (~220 nm) without growth interruption. The (010) Fe-doped Ga_2O_3 substrates were cleaned in HF for 30 mins prior to channel growth. From Hall measurements, this stack design is shown to have an effective RT Hall mobility values in the range 162 – 184 cm^2/Vs for doped channel electron densities of 1.5-3.5×10^{17} cm^{-3} measured on multiple samples/substrates. These mobility values are higher than the state-of-the-art values in Ga_2O_3 literature. Two types of (010) Fe-doped Ga_2O_3 bulk substrates were used in this study: 5×5 mm^2 diced pieces from 10×15 mm^2 EFG-grown substrates from NCT, Japan and 2-inch CZ-grown bulk substrates from NG Synoptics, USA.

The charge and transport properties were also verified using CV, TLM, field-effect mobility (μ_{FE}) measurements and FET current characteristics. Few samples were processed for regrown ohmic contacts to minimize contact resistance. R_C values of 1-2 Ω.mm were achieved. 3D electron densities were verified by CV measurements. Channel charge profile (from CV) showed the absence of any active parasitic charge below the buffer layer. R_{sh} values from TLM measurements matched closely with Hall measurements. RT μ_{FE} measured on FatFET structures (L_G ~110um, L_{GS}/L_{GD} ~ 1um) showed peak values of 158 and 168 cm^2/Vs in the doped region for electron densities of 3.5×10^{17} cm^{-3} and 2.1×10^{17} cm^{-3} respectively, which are also the highest values to be ever reported. MOSFETs and MESFETs with device dimensions $L_{GS}/L_G/L_{GD}$ = 1/2.5/5 um show max ON currents of ~200 mA/mm and ~130 mA/mm respectively. MESFETs show very high I_{ON}/I_{OFF} ~ 10^{10} and ultra-low reverse leakage. OFF-state voltage blocking capabilities of these devices will be reported.

These buffer-engineered doped high-mobility Ga_2O_3 channel layers with superior transport properties show great promise for Ga_2O_3 power devices with enhanced performance.

Acknowledgement: This material is based upon work supported by the II-VI foundation Block Gift Program 2020-2022. This material is also based upon work supported by the Air Force Office of Scientific Research under award number FA9550-21-0078 (Program Manager: Dr. Ali Sayir). We thank AFRL sensors directorate for discussions.

Electronic and Photonic Devices, Circuits and Applications
Room Jefferson 2-3 - Session EP2-WeM

Process and Devices IV

Moderator: Christina DiMarino, Virginia Tech

10:45am **EP2-WeM-10 *β*-Ga_2O_3 Lateral FinFETs Formed by Atomic Ga Flux Etching**, ***Ashok Dheenan**, N. Kalarickal, Z. Feng, L. Meng,* The Ohio State University*; A. Fiedler,* IKZ Berlin, Germany*; C. Joishi, A. Price, J. McGlone, S. Dhara, S. Ringel, H. Zhao, S. Rajan,* The Ohio State University

β-Ga_2O_3 is an ultrawide bandgap semiconductor with attractive properties for high-power electronics including a high theoretical breakdown field of 8 MV/cm and availability of melt-grown substrates. Low room-temperature electron mobility and low thermal conductivity result in both high sheet-resistance and high thermal resistance, limiting field-effect transistor performance. A 'fin' channel structure can overcome these challenges by utilizing a tri-gate geometry to enable electrostatic control over a high sheet-charge density channel while also providing additional surface area for thermal management in the active region. A key process technology for non-planar devices is a low-damage etch method. In this work, we demonstrate *β*-Ga_2O_3 lateral FinFETs with high sheet charge density fabricated with a novel damage-free atomic Ga flux etching technique [N.K. Kalarickal *et* al. APL **119** (2021)]. The epitaxial structure was grown by MOCVD on a (010) Fe-doped semi-insulating substrate. An Mg-doped layer was used to compensate Si donors at the substrate-growth interface to eliminate any parasitic channel. A 500 nm buffer layer was used to isolate the 600 nm Si-doped channel from the Mg and Fe dopants. The process flow started with selective-area MOCVD regrowth of n+ source/drain using a PECVD SiO_2 mask patterned by optical lithography and dry etching. Then a SiO_2 mask for the fins and mesa isolation layer was patterned by electron-beam and optical lithography. The sample was etched by atomic Ga flux -in an MBE chamber. Electron-beam evaporated Ti/Au ohmic contacts were annealed in an N_2 ambient. Ni gates were deposited by RF sputtering. Hall measurements revealed a sheet-charge density of 2.28x10^{13} cm^{-2}, a mobility of 134 $cm^2/V.s$ and a sheet resistance of 1.77 kΩ/sq. Transfer length method showed a contact resistance of 1.27 Ω.mm, a sheet resistance of 2.03 kΩ/sq and a specific contact resistivity of 9.11x10^{-6} $Ω.cm^2$. C-V measurements at 100 KHz were used to extract a doping density of 6x10^{17} cm^{-3} in the channel. Current density is above 250 mA/mm normalized to the total fin width for a device with a gate length of 1.5 µm and an L_{SD} of 2.5 µm. Transfer characteristics show a threshold voltage of -12 V for a fin width of 200 nm. The on/off ratio of 10^5 is limited by the reverse leakage of the Schottky gate. In summary, *β*-Ga_2O_3 FinFETs with scaled fins were fabricated using novel damage-free Ga flux etching and show promising electrical performance. We acknowledge funding from DOE/NNSA under Award Number(s) DE-NA000392 and AFOSR GAME MURI (Award No. FA9550-18-1-0479, project manager Dr. Ali Sayir).

11:00am **EP2-WeM-11 Insights Into the Behaviour of Leakage Current in Lateral Ga_2O_3 Transistors on Semi-Insulating Substrates**, *Z. Chen, A. Mishra, M. Smith, T. Moule,* University of Bristol, UK*; M. Uren,* University of Brsitol, UK*; S. Kumar,* ***Masataka Higashiwaki,*** National Institute of Information and Communications Technology, Japan*; M. Kuball,* University of Bristol, UK

Off-state leakage currents in lateral Ga_2O_3 FET devices have previously been attributed to the presence of unintentional Si (n-type) at the interface between epitaxial grown layer and the substrate [1-4], i.e., a parallel leakage conducting channel. High Fe-doping (>10^{19} cm^{-3}) at the surface of the Ga_2O_3 substrate, followed by thermal annealing, has been shown to compensate the unintentional Si impurities, thereby reducing the leakage current. However, elevated off-state currents and low on-off ratios have still been observed in these devices [4]. Here, we utilize electrical characterization and TCAD simulations to explore the behaviour of leakage current due to Si impurities at the surface of the substrate in lateral Ga_2O_3 transistors.

Lateral Ga_2O_3 transistors studied here were processed on an MBE-grown epitaxial layer on surface-implanted (Fe, p-type) semi-insulating Ga_2O_3 substrates, followed by thermal annealing (more details in ref. 4). The transfer characteristic reveals a pinch-off current (10^{-7}A/mm) with an insensitivity to the gate voltage (Fig 2(a)). The pinch-off current demonstrates ohmic characteristics under opposite drain voltage. The clockwise hysteresis in the C-V and the depletion width (Fig 3) indicate a donor-like trapping effect located near the epitaxy/substrate interface with an activation energy of 0.5eV determined by drain current transients (Fig 4).

2D TCAD simulations (Fig 5), using the SIMS profile for Fe and Si [4] as input parameters, illustrate that the residual Si at the epitaxy/substrate interface pin the Fermi level near the conduction band, resulting in the formation of a parallel conducting channel at the epitaxy/substrate interface (Fig 5(b)). Electrons, from the traps in the epilayer and the contacts, travel vertically to the parallel channel at that interface under negative gate bias. The insensitivity of the leakage current to the gate voltage can be explained by the pinning of the Fermi level due to the high concentration of residual Si dopants. The leakage current magnitude is mostly governed by the resistance of the UID Ga_2O_3 rather than the parallel conduction channel. The latter is evidenced by the constant resistance of the parallel channel in set of circular isolation structures with different spacing (Fig.6). An activation energy of 0.36eV was determined for the leakage current pathway, which contains contributions from the UID layer and the parallel channel (Fig. 7). The mechanism discussed here highlights the role of residual Si contaminants on leakage current. Reduction in their concentration or full compensation is crucial for enhancing performance and device design respectively.

11:15am **EP2-WeM-12 Device Figure of Merit Performance of Scaled Gamma-Gate β-Ga_2O_3 MOSFETs**, ***Kyle Liddy**, A. Islam, J. Williams, D. Walker, N. Moser, D. Dryden, N. Sepelak, K. Chabak, A. Green,* AFRL

The dynamic switching loss figure of merit ($R_{ON}Q_G$ vs. V_{BK}) is a benchmark used to indicate a device's potential in power-switching applications. Similarly, the lateral Power Figure of Merit ($R_{ON,sp}$ vs. V_{BK}) indicates a devices conduction losses.. This work discusses the fabrication and FOM characterization of optical gate and EBL gate Ga_2O_3 MOSFETs and shows their potential for these application spaces that are currently dominated by other technologies.

A 50 nm Si doped β-Ga_2O_3 channel layer was homoepitaxially grown on a Fe doped (010) substrate by ozone molecular beam epitaxy (MBE) targeting 1.0x10^{18} cm^{-3} carrier concentration. Device fabrication began with mesa isolation using a high-power BCl_3/Cl_2 ICP etch. Contact to the active layer was achieved with a Ti/Al/Ni/Au metal stack deposited by electron beam metal evaporation followed by a 470 ºC anneal in N_2 ambient for 2 minutes. 20 nm of Al_2O_3 gate dielectric was deposited via plasma-enhanced atomic layer deposition. Optical I-gate contacts were defined on half of the sample via optical stepper lithography followed by Ni/Au metal

evaporation. Scaled gamma-gates were defined on the remaining half via electron-beam lithography followed by Ni/Au metal evaporation. Interconnect metal was defined via stepper lithography followed by Ti/Au metal evaporation.

Gate capacitance was collected as a function of gate voltage at a frequency of 1 MHz, and can be seen for the various device types in Figures 2 A and B. Integration over the collected gate voltage range produces the experimentally extracted Q_{GS} of .0014/.0011 and .00082/.00078 nC for the optical and e-beam gate devices respectively. Q_{GD} is calculated assuming maximum depletion of the entire L_{GD}, Using the equation $Q = qN_DAT$. This provides a conservative representation of the total gate charge for these devices when $Q_G = Q_{GS} + Q_{GD}$ of .0060/.0041 nC and .0050/.0034 nC for optical and EBL gate devices respectively. Standard DC I-V device characterization was performed and is shown in Figure 3(A-F).

11:30am **EP2-WeM-13 Electromigration of Native Point Defects and Breakdown in Ga_2O_3 Vertical Devices**, *M. Haseman, D. Ramdin,* Ohio State University*; W. Li, K. Nomoto, D. Jena, G. Xing,* Cornell University*; **Leonard Brillson**,* Ohio State University

Beyond the extensive literature on the properties and applications of β-Ga_2O_3 for high power devices, the effects of strong electric fields on the Ga_2O_3 microstructure and in particular the impact of electrically active native point defects have been relatively unexplored.We used cathodoluminescence (CL) point spectra and hyperspectral imaging to observe the spatial rearrangement of oxygen vacancy and vacancy-related defects in Ga_2O_3 vertical trench devices under strong reverse bias.The low crystal symmetry of β-Ga_2O_3 leads to unequal migration of V_O and H-related defects under applied bias resulting in a preferential accumulation of donor species near trench corners where the applied field is strongest, increasing the electric field locally and likely leading to breakdown of the dielectric region.Point defect redistribution along the biasing direction demonstrate post-*operando* the reduced surface electric field (RESURF) effect modulated by the device geometry.

We used CL point spectra and HSI mapping to demonstrate how point defect related donor species in β-Ga_2O_3 vertical Schottky diodes migrate and redistribute under high reverse electrical bias.The accumulation of donor-related defects at Schottky barrier trench corners increases the local doping density and decreases the Ga_2O_3 depletion width such that the electric field falls across a narrower total insulator region, thereby increasing the field locally in the nanoscale trench corner.The low crystal symmetry of the monoclinic crystal structure results in unequal migration energies for point defects on inequivalent lattice sites and along inequivalent crystallographic directions, suggesting a preferential migration of specific three-fold coordinated oxygen vacancies and/or migration of positively charged hydrogen species, altering the relative intensity of the UV emissions that we observe via spatially resolved CL maps and linecuts.Together with the local electrical field maximum under reverse bias resulting from the fin/trench design, this local doping increase due to defect migration suggests a point-of-failure near the trench corners. More generally, defect migration and local doping changes under extreme electric fields in β-Ga_2O_3 demonstrates the potential impact of nanoscale device geometry in other high-power semiconductor device structures.

This work supported by AFOSR grant FA9550-18-1-0066 and NSF grant DMR-18-00130.This work also supported by AFOSR under Grant FA9550-18-1-0529 and made use of the Cornell Center for Materials Research Facilities supported by NSF MRSEC program (DMR-1719875).

Author Index

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