

Reference

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- [3]. T. J. Asel; et al.; J. Vac. Sci. Technol., A 38, 043403 (2020).
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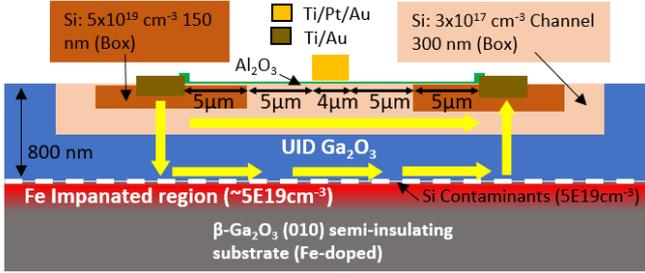


Fig 1 Device schematic with current flow paths. There is parallel leakage path at the epilayer/substrate interface.

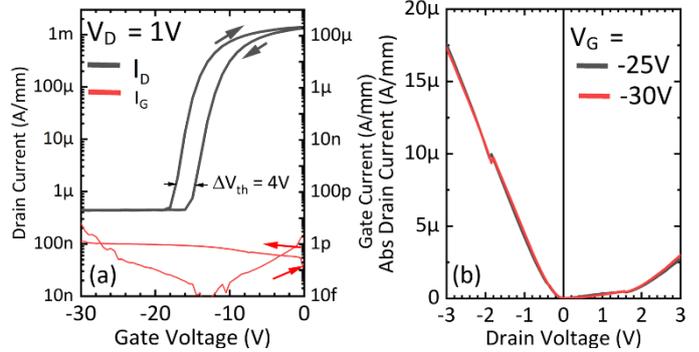


Fig 2 (a) Transfer characteristics and **(b)** pinch-off current with drain voltage between -3V and +3V.

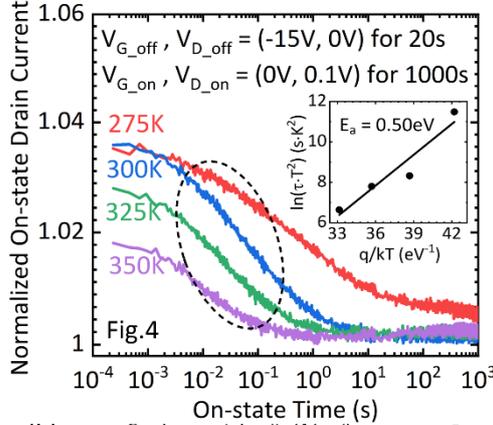
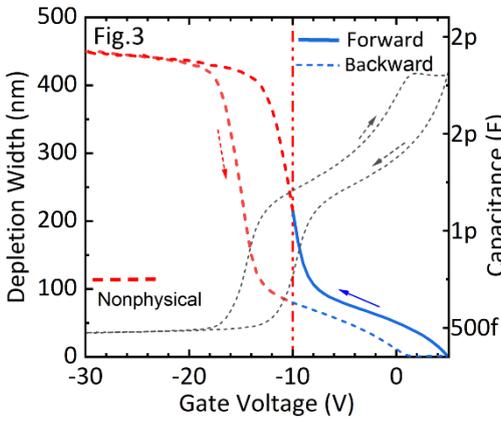


Fig 3 Depletion width calculated from C-V measurements $V_G = -10V$ is corresponding to $\sim 250nm$ below gate oxide, which near the channel/UID interface

Fig 4 Drain current transient for on-state current with -15V off-state stress. Inset illustrates an activation energy of 0.50eV.

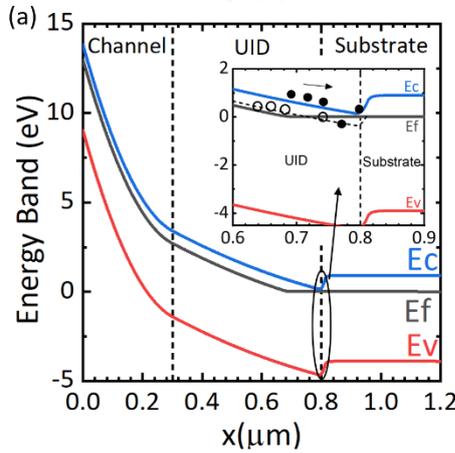


Fig 5. Drift diffusion simulation results of the lateral Ga_2O_3 transistor under $V_G = -15V$ and $V_D = 0.1V$ (a) Band diagram underneath gate. (b) Current density and the electron concentration

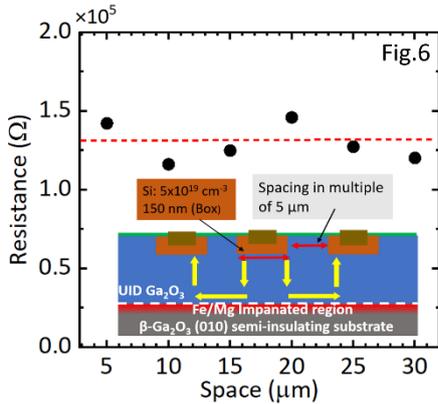


Fig 6 Resistance of isolation structure with different spacings.

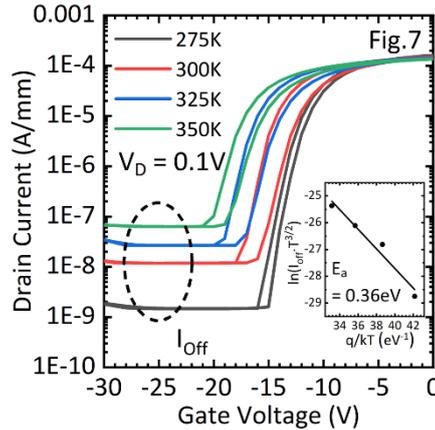


Fig 7 Transfer characteristics in different temperature. Inset illustrates an activation energy of leakage current, which is 0.36eV