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## Keynote Address
## Room Jefferson 2-3 - Session KEY1

### Keynote Address

**Moderator: Dr. Kelson Chabak**, Air Force Research Laboratory

8:45am **KEY1-2 Keynote Lecture: $Ga_2O_3$ Device Technologies: Power Switching and High-Frequency Applications, and Beyond***, Masataka Higashiwaki,* Department of Physics and Electronics, Osaka Metropolitan University, Japan*; T. Kamimura, S. Kumar, Z. Wang,* National Institute of Information and Communications Technology, Japan*; T. Kitada, J. Liang, N. Shigekawa,* Department of Physics and Electronics, Osaka Metropolitan University, Japan*; H. Murakami, Y. Kumagai,* Department of Applied Chemistry, Tokyo University of Agriculture and Technology, Japan **INVITED**

Developments of $Ga_2O_3$ field-effect transistors (FETs) and diodes are being actively conducted all over the world. From the world-first demonstration of single-crystal $Ga_2O_3$ FETs in 2011 [1], we have been developing both vertical and lateral $Ga_2O_3$ devices. In this talk, our latest selected challenges on vertical $Ga_2O_3$ Schottky barrier diodes (SBDs), vertical Si/$Ga_2O_3$ heterostructures, and lateral short-gate $Ga_2O_3$ FETs will be discussed.

$Ga_2O_3$ SBDs with a trench staircase field plate were fabricated [2]. We found that the staircase field plate on the deep trench filled with $SiO_2$ can effectively alleviate electric field concentration in both the $Ga_2O_3$ drift layer and the $SiO_2$. The $Ga_2O_3$ SBDs successfully demonstrated superior device characteristics including an on-resistance of 7.6 $m\Omega cm^2$ and an off-state breakdown voltage of 1.66 kV.

Next, our pioneering work on vertical n-Si/n-$Ga_2O_3$ heterostructures fabricated using surface-activated bonding will be presented [3]. Analyses of temperature-dependent current density–voltage characteristics of the heterostructures revealed that an energy barrier was formed at the Si/$Ga_2O_3$ heterojunction interface due to negatively charged interface states. The conduction band offset at the bonding interface was estimated to be 0.18 eV.

We have also been developing lateral $Ga_2O_3$ FETs with a highly scaled gate for high-frequency and logic applications in harsh environments. Submicron-gate $Ga_2O_3$ FETs with a thin channel layer formed by Si-ion implantation doping achieved promising device performance typified by a maximum oscillation frequency of 27 GHz at a gate length of 200 nm [4].

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[1] M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, Appl. Phys. Lett. **100**, 013504 (2012).

[2] S. Kumar, H. Murakami, Y. Kumagai, and M. Higashiwaki, Appl. Phys. Express, *in press*.

[3] Z. Wang, D. Takatsuki, J. Liang, T. Kitada, N. Shigekawa, and M. Higashiwaki,J. Appl. Phys. **131**, 074501 (2022).

[4] T. Kamimura, Y. Nakata, and M. Higashiwaki, Appl. Phys. Lett. **117**, 253501 (2020).

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