Program Overview

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Electronic and Photonic Devices, Circuits and Applications
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Electronic and Photonic Devices, Circuits and Applications Poster Session

EP-MoP-2 Gate Effects of Channel and Sheet Resistance in β-Ga_2O_3 Field-Effect Transistors using the TLM Method, ***Ory Maimon***, Department of Electrical Engineering, George Mason University; *N. Moser,* Air Force Research Laboratory, Sensors Directorate; *K. Liddy, A. Green, K. Chabak,* Air Force Research Laboratory, Sensors Directorate, USA; *C. Richter, K. Cheung, S. Pookpanratana,* Nanoscale Device and Characterization Division, National Institute of Standards and Technology; *Q. Li,* Department of Electrical Engineering, George Mason University

Beta Gallium Oxide (β-Ga_2O_3) is a rapidly developing semiconductor for high power electronic devices with promising advantages. Accurate characterization of the resistances in β-Ga_2O_3 field-effect transistors (FET) are critical to understand and model these devices. Here, we report on extracting contact, channel, and sheet resistances from planar, depletion-mode β-Ga_2O_3 FETs using the transfer length method (TLM). The results are analyzed in comparison with conventional TLM structures fabricated on the same wafer. The β-Ga_2O_3 FETs are composed of a 50-nm Si-doped epi-layer with a target concentration of 2.4 x 10^{18} cm^{-3} fabricated on a (010) semi-insulating β-Ga_2O_3 substrate. Aluminum oxide (Al_2O_3, 20 nm) was used as the gate dielectric and the gate length (L_G) remained constant at 1.94 µm, while the source-drain spacing (L_{SD}) varied as 3µm, 8 µm, and 13 µm. No back contact was used due to the semi-insulating substrate. Transfer characteristic measurements were taken at room temperature and low drain-source voltage (V_{DS}) of 0.01 V to suppress drain effects on the threshold voltage (V_{TH}), about -4 V, for devices at different L_{SD} spacing.

When compared to the TLM structures, we observe a decrease in extracted sheet resistance (R_{sh}), and channel sheet resistance (R_{ch}) as the channel turns on with increasing gate-source voltage (V_{GS}). The contact resistance (R_C) is assumed to be constant, and is found to be 27.7 Ω mm at a V_{GS} of 0 V. From a V_{GS} of -3 V to 3 V (off to on state), R_{sh} quickly decreases from 90.4 kΩ sq^{-1} and appears to plateau at 28.2 kΩ sq^{-1}. We saw a similar trend for R_{ch}, which decreased from 288 kΩ sq^{-1} to 7.66 kΩ sq^{-1}. From the channel sheet resistance, we can find an accurate field-effect mobility after removing the parasitic resistances. A FET with an L_{SD} of 3µm was found to have a field-effect mobility of 61 cm^2 V^{-1} s^{-1} at a V_{GS} of 3 V. This work indicates that the channel resistance can be accurately extracted by applying the TLM method to FETs, and further helps understand β-Ga_2O_3 gate effects on transistor performance.

EP-MoP-3 Lateral β-Ga_2O_3 Schottky Barrier Diodes With Interdigitated Contacts, ***Jeremiah Williams***, Air Force Research Laboratory, Sensors Directorate; *A. Arias-Purdue,* Teledyne; *K. Liddy, A. Green,* Air Force Research Laboratory, Sensors Directorate; *D. Dryden, N. Sepelak,* KBR; *K. Singh,* Air Force Research Laboratory, Sensors Directorate; *F. Alema, A. Osinsky,* Agnitron Technology; *A. Islam, N. Moser, K. Chabak,* Air Force Research Laboratory, Sensors Directorate

This work characterizes a lateral β-Ga_2O_3 Schottky barrier diode (SBD) with an interdigitated contact design fabricated using a homoepitaxial thin-film. This SBD design can be monolithically integrated into RF power switching circuits with standard lateral FET processing. This technique avoids complex fabrication and losses from heterogeneous integration while maintaining the fast switching capabilities of a thin, lateral channel. Prior literature has shown impressive performance from vertical SBDs [1] and lateral devices on non-native substrates [2], but lateral SBDs on homoepitaxial β-Ga_2O_3 thin-films are not well explored. To the authors' knowledge, this is the first demonstration of such a SBD design in β-Ga_2O_3.

The β-Ga_2O_3 epitaxial layer is grown by MOCVD with a target thickness of 65 nm. Hall effect measurements indicate Si doping of 3.347e17 cm^{-3}, carrier mobility of 86.5 cm^2/V-s, and a sheet resistance of 33.15 kΩ/sq. A surface RMS roughness of 0.839 nm is measured by AFM. Mesa isolation is achieved with a BCl_3 ICP etch. Ohmic contacts are formed by Si ion implantation and a metal stack of Ti/Al/Ni/Au (25/120/50/50 nm) annealed at 470°C. Implant carrier concentration is measured at 5.976×10^{19} cm^{-3}. Evaporated Pt/Au (20/380 nm) forms the Schottky contact. The first passivation layer is 30 nm of Al_2O_3 deposited by ALD patterned with BOE. Next, a metal interconnect layer of Ir/Au (10/380 nm) is deposited. Final passivation is ~85 nm of Al_2O_3 by ALD pattered with a CF_4 RIE etch. All metal is pattered by photoresist lift off.

The diode features four 4x50 µm anode fingers interdigitated with five 8x50 µm cathode fingers. The anode-cathode spacing is 5 µm. The Pt-Ga_2O_3 barrier height is extracted from temperature dependent J-V measurements to be 1.742 eV. Fitting to forward bias J-V measurements shows an ideality factor of 2.246 and a build-in voltage of 1.963 V. The diode has a breakdown voltage (V_{bk}) of 784 V and a specific on-resistance ($R_{on,sp}$) of 9.133 Ω-cm^2, normalized to the current carrying region between contacts. This yields a power figure of merit (PFOM) of 67.3 MW/cm^2. We attribute the poor ideality to the highly resistive epitaxy and the degraded interface caused by the relatively rough surface. This device is competitive with published lateral SBD results, and establishes a baseline to enable further development of β-Ga_2O_3 RF power switching circuits with a streamlined, monolithic fabrication process.

[1] S. Roy *el al.*, *IEEE Electron Device Lett.*, **34**, 8, (2021).

[2] Z. Hu *et al.*, *IEEE Electron Device Lett.*, **39**, 10, (2018).

EP-MoP-4 Optimized Annealing for Activation of Implanted Si in β-Ga2O3, ***Katie Gann***, *J. McCandless,* Cornell University; *T. Asel, S. Tetlak,* Air Force Research Laboratory; *D. Jena, M. Thompson,* Cornell University

Ion implantation of β-Ga_2O_3 will be critical for low resistance contacts and advanced device structures. Literature suggests good activation of Si implants after annealing under N_2, but reversible deactivation of carriers under O_2-rich annealing. However, there have been no significant studies establishing annealing behavior as a function of time, temperature, and controlled gas ambients. Unintentionally doped (UID) β-Ga_2O_3 films, grown by plasma assisted molecular beam epitaxy on Fe-doped semi-insulating β-Ga_2O_3 substrates with a UID thickness >400 nm, were ion implanted with Si to a total dose of 7x10^{14} cm^{-2} at three energies (15-115 keV) through an SiO_2 cap (20 nm) to yield a 100 nm box profile with a concentration of 5x10^{19} cm^{-3}. Secondary ion mass spectrometry (SIMS) was used to compare implant profiles to SRIM simulated ion ranges, and to quantify Si diffusion during annealing. A wide range of annealing conditions were studied using a load-locked ultrahigh vacuum compatible quartz tube furnace with precise gas control. Anneal times were varied from 10 to 120 minutes, temperatures from 850 to 1000 °C, and the anneal ambient gas was varied by mixing research plus (RP) N_2 with ultra-high purity (UHP) O_2 to control the oxygen partial pressure (pO_2) between <10^{-6} and 1.0 bar. Gases were also selectively passed over a desiccant to reduce the water vapor partial pressure to <10^{-8} bar. Sheet resistance, carrier activation, and mobility were determined using van der Pauw structures. Annealing in extremely low pO_2 (forming gas 4% H_2/N_2) resulted in decomposition of the Ga_2O_3, while annealing at pO_2 above 10^{-2} bar resulted in minimal carrier activation. Within the moderate pO_2 range, minimizing the partial pressure of water vapor was shown to be critical to achieve high carrier activation, with the negative impact of water vapor becoming more significant with increasing pO_2. Data, however, suggests that a trace level of water vapor may slightly improve carrier activation.Short duration anneals resulted in higher carrier activation with longer times resulting in "over annealing" and reduced carrier density. Optimal anneal temperatures were determined to be between 900 and 950 °C, with lower temperatures showing reduced mobility and higher temperatures exhibiting reduced carrier activation and increased Si diffusion. The optimized anneal conditions for this implant were found to be at 950 °C for 20 minutes under dried RP N_2, with an extended gas purge of the furnace prior to the anneal to remove any residual water vapor, resulting in 88% carrier activation and a mobility of 72 cm^2/V-s (R_s = 130 Ω/sq).

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