Advanced Packaging
Room Ballroom A - Session PK-ThP

Advanced Packaging Poster Session

PK-ThP-1 A Numerical Investigation of Acoustic Void Detection in Through Silicon Vias using the Rayleigh-Ritz Method, ***George Antonelli***, Antonelli Research & Technology; *Shiva Mudide,* Massachusetts Institute of Technology

Voids formed in through silicon vias (TSVs) during metallization pose significant reliability risks and are challenging to detect using conventional optical, x-ray, and electron beam defect inspection and review techniques. Non-destructive acoustic approaches such as scanning acoustic microscopy (SAM) and photoacoustics have been proposed to fill this gap. The expected signals from voided TSVs can be investigated with mechanical simulations using the finite element method to guide the development of hardware; however, these calculations can be slow and tedious to setup. We propose the application of a frequency-domain modeling framework based on the Rayleigh–Ritz variational method. Closed-form expressions for monomial volume moments can be derived for spherical, conical, cylindrical, and composite voids, enabling rapid parametric evaluation of void-induced perturbations to the vibrational spectrum. Symmetry constraints imposed by photoacoustics and SAM excitation conditions reduce the accessible mode space, further reducing the complexity of the calculation. Numerical studies demonstrate strong mode-specific sensitivity to void size and shape and reveal the dominant influence of geometric parameters—such as aspect ratio and radius—on modal dispersion.

Advanced Packaging
Room 304 - Session PK+MS-FrM

Advanced Packaging Oral Session

Moderators: Dr. Mohanalingam Kathaperumal, Georgia Institute of Technology, USA, **Dr. John Lannon**, Micross, **Dr. Prahalad Murali**, AMD

8:15am **PK+MS-FrM-1 Advances Packaging Approaches for Chiplet Solutions**, ***Tanja Braun***, Fraunhofer IZM, Germany **INVITED**

The economic advantages of silicon scaling according to Moore's Law have gone, as today, only a limited number of foundries can afford the manufacturing of high-end nodes. Now, heterogeneous integration in combination with advanced packaging are the path to achieve economic advantages and also to enable new applications. Many options for the package including silicon interposers, Fan-out on substrate, bridge solutions and variations of 3D stacking approaches are seen as possible solutions. However, performance of current applications requires still more transistors per system, but industry also needs a new, more economical system packaging approach. Chiplets are considered the main solution to address this challenge.

Besides all the design aspects, packaging of Chiplet-based systems also holds quite some challenges and requires advanced packaging approaches. The presentation will summarize different advanced packaging solutions as Flip Chip on organic, silicon or fan-out interposer and discuss key challenges as e.g. warpage and possible mitigation solutions. In summary the entire packaging approach from chip to system board has to be considered.

8:45am **PK+MS-FrM-3 Advanced Packaging Enables the Future of the Semiconductor Industry**, ***Charles Woychik***, NHanced Semiconductors, Inc.

The semiconductor industry has long relied on Dennard scaling and Moore's Law to drive advancements in performance and cost efficiency. Dennard scaling asserts that as transistors shrink, power density remains constant, allowing for faster clock speeds and more transistors per unit area without increased power consumption. Moore's Law predicts the doubling of transistors on a chip approximately every two years, leading to exponential growth in computing power. However, as these principles reach their physical and economic limits, the industry faces escalating challenges. Shrinking transistors further is becoming increasingly difficult and expensive due to quantum effects, power leakage, and escalating fabrication costs. Consequently, advanced packaging (AP) technologies have emerged as pivotal in continuing the trajectory of semiconductor innovation.

AP refers to techniques that integrate multiple semiconductor chips into a single package, enhancing performance, power efficiency, and functionality without solely relying on further transistor miniaturization. Methods such as 3D stacking, system-in-package (SiP), and heterogeneous integration (HI) allow for the combination of different types of chips—each optimized for specific functions—into compact, efficient systems. This approach not only mitigates the limitations of traditional scaling but also enables enhanced connectivity, reduced latency, and improved thermal management. By leveraging advanced packaging, the semiconductor industry can continue to innovate, meeting the growing demands for higher performance and efficiency in applications such as artificial intelligence, high-performance computing, and telecommunications. In this presentation, an overview of our 3 families of Si and glass interposers will be presented along with our hybrid bonding capabilities to achieve the aggressive future demands for AI generative computing.Examples will be presented that use these core AP/HI technologies to achieve the aggressive requirements for AI generative computing.

9:00am **PK+MS-FrM-4 Heterogeneous Integration Enabled by Fanout Wafer Level Packaging Prototyping Facility and Activities at Arizona State University**, ***Hongbin Yu***, Arizona State University

Advanced packaging and integration have received increasing attention as computing and communication systems have become more sophisticated and ubiquitous, from CPU/GPU integration with HBM for AI application to III-V power and communication chips integrated with Si COMS chips. Fanout wafer level packaging (FOWLP) has become a versatile and capable technology that enables such heterogenous integration (HI). At Arizona State University, a 300 mm FOWLP prototyping line is being established that is aimed for facilitation advanced packaging research and development as well as demonstration. Examples from Southwest Advanced Prototyping (SWAP) Hub and Department of Commerce funding advanced substrate program SHILED will be discussed.

9:15am **PK+MS-FrM-5 Maskless Lithography for Wafer and Panel-Level Advanced Packaging: Enabling Adaptive Patterning Beyond Reticle Limits**, ***Jonas Wiedenmann***, Heidelberg Instruments Mikrotechnik GmbH, Mittelgewannweg 27, 69123 Heidelberg, Germany **INVITED**

The continued evolution of advanced semiconductor packaging is driven by increasing demands for higher data rates and bandwidth in artificial intelligence- and high performance computing-oriented devices. As a result, package sizes are growing while line and space requirements are becoming more stringent. Traditional mask-based lithography approaches face fundamental limitations as substrate dimensions exceed reticle boundaries. At the same time, warpage, distortion, and non-uniform topography introduce additional challenges for pattern fidelity and manufacturing yield.

Maskless lithography has emerged as a promising enabling technology for next-generation advanced packaging, particularly for panel-level and large-format applications. By eliminating the need for masks and enabling direct-write patterning, maskless approaches offer unique advantages in flexibility, scalability, and cost efficiency. In particular, adaptive patterning strategies—enabled by real-time design data corrections—provide new pathways for compensating substrate distortion, local warpage, and process-induced variations.

This presentation will provide an overview of maskless lithography in the context of advanced packaging applications, including redistribution layers (RDL) and substrate patterning. Key capabilities such as high-resolution patterning down to the 1–2 µm line/space regime, as well as seamless patterning across large areas through stitching, will be discussed.

The second part of the talk will focus on grayscale lithography and its applications in co-packaged optics. A key challenge in this domain is the fabrication of large-area flat optical elements. Using a newly developed grayscale process, it will be demonstrated how such structures can be realized without introducing unwanted step artifacts. Additional applications of direct laser writing for co-packaged optical systems will also be addressed.

9:45am **PK+MS-FrM-7 Development of a Domestic Fan-Out Wafer-Level Packaging Platform for Advanced Heterogeneous Integration**, ***James Will***, SkyWater Technology

Advanced packaging has become a critical enabler for heterogeneous integration in applications spanning defense and aerospace, telecommunications, high-performance computing, and artificial intelligence. While substantial investments are being made to strengthen domestic semiconductor manufacturing, advanced packaging capabilities remain limited within the United States. To address this gap, SkyWater Technology is establishing a domestic fan-out wafer-level packaging (FOWLP) manufacturing capability to support secure, scalable integration of advanced semiconductor devices.

This work presents the development of key process modules required for implementation of a 300 mm FOWLP platform capable of integrating multiple die within high-density chip-scale packages (CSP) and multi-chip modules (MCM). The process flow leverages adaptive patterning technology to compensate for die placement variation and enable fine-pitch redistribution layer (RDL) interconnects for heterogeneous integration beyond conventional reticle limitations.

Results from process module development and integration activities are presented, including die placement and molding processes, wafer reconstitution, dielectric deposition and patterning, copper redistribution layer fabrication, and process characterization supporting fine-line interconnect formation. Particular emphasis is placed on achieving high-yield pattern fidelity, overlay control, and electrical continuity across large-area reconstituted wafers. Development efforts supporting fine-pitch interconnect architectures, including line/space dimensions approaching 1.5 µm and die I/O pitch down to 20 µm, are discussed along with associated metrology and defectivity reduction strategies.

The presentation will further describe process integration challenges encountered during establishment of a domestic FOWLP manufacturing line and the approaches used to improve manufacturability, scalability, and reliability. Early electrical, physical, and reliability characterization data from engineering test structures and package demonstrators will be reviewed. In addition, development activities supporting future expansion to dual-side fan-out architectures, including through-mold vertical interconnect technologies for enhanced power delivery and signal integrity, will be discussed.

These results demonstrate progress toward establishing a trusted domestic FOWLP capability and provide insight into the process technologies

required to enable next-generation heterogeneous integration solutions for national security and other critical applications.

10:00am **PK+MS-FrM-8 SCAPEx: Status of Onshoring Secure 300mm Wafer Bumping and TSV Wafer Finishing***, **Rex Anderson**, John Lannon,* Micross Advanced Interconnect Technology LLC

The Reshore Ecosystem for Secure Heterogeneous Advanced Packaged Electronics (RESHAPE) program is tasked with ensuring the defense industrial base (DIB) has access to a secure, domestic advanced packaging, assembly, and test capability. As part of that program, the Micross Advanced Interconnect Technology business unit in North Carolina has been funded to establish 300mm wafer bumping and 300mm wafer preparation (wafer finishing) capabilities in its post-CMOS wafer processing facility. This paper will provide an overview of the RESHAPE program and the advanced packaging capabilities that are deployed and those that will be deployed at Micross as part the RESHAPE program.

10:30am **PK+MS-FrM-10 On-Shore Sustainable Organic IC Substrate (ICS) Fabrication***, **Michael Gleason**,* GreenSource Fabrication **INVITED**

GreenSource Fabrication's (GSF) proposal to the US government under the Defense Production Act Title III authorization was titled SOTA (**S**tate-of-the-Art) **O**nshore **A**dvanced **P**ackaging **P**roduction or SOAPP.With the help from funding provided by Federal and State resources, GSF is currently in the process of standing up a High-Density Build-Up (HDBU) facility focused on organic IC Substrate and Substrate-Like Printed Circuit Board (SLP) production.GSF's greenfield project includes world class processing tools, advanced automation and a patented generation III Aqua Regen Kinetics Zero Liquid Discharge (ZLD) wastewater treatment system.The facility will be open to serve both the DIB and commercial clients alike who have sustainable, high-mix, low to medium volume requirements which cannot be served well by larger offshore suppliers.Status and timeline of the project will be presented as well as project risks, demand, supply chain vulnerabilities, targeted technology offerings and future state.

11:00am **PK+MS-FrM-12 Impact of Formic Acid Distribution on Fluxless Reflow: Enhancing Process Uniformity and Performance***, **XINXUAN TAN**, Chen Fang, Zulal Tezcan, Purnima Narayanan, Zia Karim,* Yield Engineering System Inc.

Advanced fine-pitch fluxless solder reflow has become increasingly sensitive to both thermal and chemical process variations as bump pitch approaches 10µm and below. Previous studies demonstrated the correlation between reflow defects, process window optimization, and formic acid reduction mechanisms.

In this work, we investigate the impact of formic acid flow distribution and vapor transport on thermal uniformity and process stability in vacuum fluxless reflow processing for advanced AI chip and panel-level packaging applications. The study focuses on three critical process specifications: (1) the impact of formic acid on within-wafer (WiW) and panel-in-panel temperature uniformity, (2) process window stability, and (3) SnO/tin-formate byproduct residue control.

A vacuum fluxless reflow platform with dynamically controlled pure formic acid vapor delivery was utilized to study the interaction between gas flow distribution, thermal behavior, and byproduct transport. Process simulations were conducted to evaluate formic acid distribution, gas recirculation regions, temperature gradients, and tin-formate byproduct concentration behavior inside the process chamber. Experimental studies were performed using multiple combinations of formic acid flow, vapor distribution conditions, soak temperature, and reflow process parameters. Thermal uniformity was monitored using pyrometer and thermocouple measurements, while SEM, XPS, optical microscopy, and AOI inspections were used to characterize reflow quality, residue formation, and process window stability.

Results demonstrate that formic acid distribution directly impacts both reaction kinetics and local thermal behavior during soak and reflow processes. Higher formic acid flow improved oxide reduction efficiency but also increased localized thermal gradients and Sn-formate residue accumulation in gas recirculation regions. By optimizing formic acid flow distribution and vapor transport behavior, improved vapor mixing uniformity and byproduct removal capability were achieved while maintaining sufficient oxide reduction performance.

The optimized process demonstrated improved within-wafer and panel-in-panel temperature uniformity, expanded stable process window margins against under- and over-reflow conditions, and reduced SnO/tin-formate residue. High-yield defect-free microbump reflow performance was achieved for advanced AI chip and panel-level packaging applications. This work demonstrates that balancing formic acid reduction chemistry, thermal uniformity, and byproduct transport is critical for enabling stable high-volume vacuum fluxless reflow manufacturing for next-generation advanced packaging technologies.

11:15am **PK+MS-FrM-13 Bilayer Liners for Through Glass Vias with PVD and ALD Deposited Seed Layer and Fully Copper Plated Vias***, **Meghna Narayanan**, Mohanalingam Kathaperumal, Mark Losego,* Georgia Institute of Technology, USA

As glass packaging gains traction for next generation heterogenous integration, through glass vias (TGVs) face a critical reliability challenge arising from the large mismatch in the coefficient of thermal expansion (CTE) between glass and copper. Thermally induced stresses generated during processing and operation can lead to crack initiation in the glass substrate and eventually cause copper delamination, with the severity of failure increasing with increase in copper thickness. Mitigating these thermos – mechanical reliability concerns thus, becomes essential for the successful deployment of glass – based packaging technologies.

This work explores a bilayer liner approach for stress mitigation in TGVs, by combining the advantages of inorganic and polymeric materials. While polymer liners offer low elastic modulus and improved stress buffering, they duffer from relatively higher CTE and limited adhesion to glass. To address these limitations, a hybrid bilayer consisting of silicon oxynitride (SiOxNy) and Parylene C is investigated. SiOxNy serves as the interfacial adhesion promoting inorganic layer due to its strong adhesion to glass (8 N/cm) and compatibility with subsequent polymer deposition, while Parylene C, with it lower adhesion strength (5.3 N/cm) provides mechanical compliance provides mechanical compliance for stress relaxation. Conformal deposition of SiOxNy and Parylene C is achieved by PECCVD and CVD, respectively. Bilayer thicknesses are characterized using confocal fluorescence imaging, leveraging the distinct fluorescence responses of the two materials for independent thickness evaluation.

In parallel, this work investigates seed layer strategies for copper metallization in TGVs, comparing conventional sputtered titanium/copper seed layers with conformal platinum seed layers deposited by atomic layer deposition (ALD). As the aspect ratio of TGV increases, achieving uniform seed coverage becomes a significant challenge. Copper filling is performed through electroplating, and via fill quality is evaluated using non-destructive X-ray imaging.

This presentation will discuss the integration of hybrid liners with advanced seed layer approaches for reliable TGV metallization. Interface chemistry, morphology, and structural integrity will be examined using XPS, FIB cross section, Raman spectroscopy, while highly accelerated stress testing will be used to evaluate adhesion and failure behavior across the multilayer interfaces.

11:30am **PK+MS-FrM-14 Thin Film Characterization and Mechanisms EnablingExtreme Laser Lift-off (LLO)***, **Joshua Peck**,* Tokyo Electron America Inc.,

Fusion and Hybrid permanent wafer bonding are essential for 3D high density packaging. To enable scaling for AI applications that require multiple hybrid bonds such as HBM (high bandwidth memory). Conventional thinning processes use deionized water for contact-dependent removal, which reduces wafer yield. To address this yield loss, Tokyo Electron has developed a laser lift-off (LLO) tool that reduces water consumption by 90%. LLO enables wafer separation of fusion or hybrid bonded wafers by inorganic dielectrics. Although full-wafer LLO is novel, it remains a relatively new technology. For effective carrier wafer separation, the properties of the films that enable lift off are characterized then related to defects that may occur without an optimization. Moreover, with an optimized release process the top carrier wafer may be reworked to enable multiple uses of the same carrier wafer.

To enable LLO and wafer reuse, the film properties have been characterized. This characterization covers how increasing laser energy affects wafer bow, how decreasing laser fluence reduces surface roughness, and the films' thermal response from 500-800°C. The challenges associated with carrier wafer integration after LLO will be addressed.

Keywords: laser lift-off, topology, AVS

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Figure #1: As Laser pitch increases RMS roughness (Rq) exponential decreases do to low fluence.

Figure #2: Simulation of stress on engineered thin films during LLO

11:45am **PK+MS-FrM-15 Plasma Surface Engineering for Low Distortion Wafer Bonding**, ***Andrew Tuchman***, *Christopher Netzband, Joshua Greklek, Nathan Ip, Ilseok Son,* Tokyo Electron America, Inc.

Low distortion wafer-to-wafer bonding is a critical technology for several advanced logic and memory architectures including backside power delivery network (BSPDN) and $4F^2$ DRAM. These process flows require a direct wafer bonding step to transfer a patterned device layer to a separate blanket carrier wafer with less than 5nm of pattern distortion after higher order lithography alignment and correction. In this work we explore the impact of the wafer bonding surface chemistry on the post-bond distortion of SiO_2 bonding dielectrics. A nitrogen-based RF surface activation plasma was used to modify the SiO_2 surface prior to bonding with several plasma conditions. A direct correlation was made between surface nitrogen concentration as measured by XPS and post-bond distortion, with higher nitrogen concentration providing lower post-bond wafer warpage and distortion. Higher surface nitrogen content replaces the hydrophilic -(OH) and dangling Si bonds on the surface, reducing the adhesion energy during bonding and lowering the post-bond warpage. Additionally, the surface nitrogen concentration on the SiO_2 bonding dielectric could be controlled through several plasma parameters. However, the final bond strength was also directly reduced at higher surface nitrogen concentrations, creating a tradeoff between lower distortion and bond strength. By tailoring the plasma conditions to maximize the surface nitrogen concentration, the post-bond distortion was reduced by 27% compared to baseline conditions. Finally, machine learning algorithms were used to determine the optimal plasma parameters for high surface nitrogen concentration with minimized variation across the full wafer. These results highlight the importance of surface-plasma engineering in low distortion bonding flows.

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