Advanced Microelectronic Materials and Devices Mini-Symposium
Room 318 - Session AM2+EM+TF-FrM

Devices II

Moderators: Dr. Samantha Jaszewski, Sandia National Labs, **Somil Rathi**, Arizona State University

10:30am **AM2+EM+TF-FrM-10 Development of Metallic Gate Stacks at Atomic Scale : Application to Advanced FD-SOI Transistors**, ***Elouan Le Cun***, *Julien Patouillard, Rémy Gassilloud, Mathieu Bernard, Zdenek Chalupa, Krunoslav Romanjek, Wissem Baik, William Vandendaele, Elhadji-Alhousseyni Diallo, Tadeu Mota Frutuoso, Pauline Hauchecorne, Virginie Loup, Théo Cabaret, Frédérique Glowacki, Mouaad Yassine Aliouat, Elise Arnoux, Gennie Garnier, Marie-Claire Cyrille, Olivier Renault, Claire Fenouillet-Béranger,* CEA-LETI, France

Fully-Depleted Silicon On Insulator (FDSOI) planar technology - an alternative to FinFET (3D field effect transistors) - address technologies involving very high energy efficiency, ultralow power consumption and cost reduction. 10 nm FD-SOI transistor requires complex metal on insulator (MOS) gate stacks. The MOS structure is composed of doped titanium nitride layers as metal gates, and SiON/HfON as gate-dielectric[1]. SiON is also called gate interlayer (IL). Thinning TiN layers results in better MOS performances. This is due to a known phenomenon called IL scavenging, where TiN acts as an oxygen reducer of the IL, which in turn reduces the IL thickness[2]. The targeted TiN thickness in the 10 nm-node FDSOI is closed to 2 nm, and the required equivalent oxide thickness (the electrical thickness of the IL/HfON insulator stack) is below 0,8 nm. As the layers thicknesses reach the nm-scale, it introduces new challenges regarding the electrical behavior of the MOSFET due to the heterogeneity of the materials in the gate stacks.

To address those challenges, the developments of an ultra-thin 2 nm metallic gate stack with sub-stoichiometric titanium nitride ($TiN_{x<1}$) are required. CEA-Leti has acquired a PVD deposition tool by co-sputtering to deposit complex metallic layers on 300 mm silicon wafers with an atomic-scale thickness control.

This study examines TiN_x ultra-thin films with thicknesses below 5 nm. TiN_x structural, optical and electrical properties are evaluated by X-Ray Reflectivity (XRR), stress measurements, sheet resistance measurements, spectroscopic ellipsometry, X-Ray Photoelectron Spectroscopy (XPS) and X-Ray Diffraction (XRD). TiN_x layer composition is investigated by Elastic Recoil Detection Analysis (ERDA) and X-Ray Fluorescence (XRF) analysis. Those layers have been integrated on simplified electrical devices to evaluate their impact on transistor key performance parameters (EOT, Vt, Jg, ...).

This work was carried out in the framework of the FAMES Pilot Line of the Chips JU and the Platform for Nanocharacterisation (PFNC) funded by Horizon Europe grant 101182279, ANR NextGen project ANR-22-NEXTG-001, ANR programs “Recherche Technologique de Base” and "France 2030 - ANR-22-PEEL-0014".

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References:

[1] C. Fenouillet-Beranger, et al, “Pursuing the FD-SOI roadmap down to 10 nm and 7 nm nodes for high energy efficient, low power and RF/mmWave applications,” Solid-State Electron. 231, 109264 (2026).

[2] T. Ando et al., Ultimate Scaling of High-κ Gate Dielectrics: Higher-κ or Interfacial Layer Scavenging, Materials 2012, 5, 478-500

10:45am **AM2+EM+TF-FrM-11 Towards Ordered Growth of Complex Oxide Thin Films for Memristive Devices**, ***Michael Mitchell***, *Xianchao Dong, Shweta Joshi, Tianshu Li, Gina Adam,* George Washington University

We present progress towards the ordered growth of the entropy-stabilized oxide, $(MgNiCoCuZn)_{0.2}O$, via reactive magnetron sputtering for the fabrication of memristive devices. To produce this film, the authors leveraged a custom-designed AJA ATC system with off-axis capabilities to reduce deposited atom kinetic energy and improve film crystallinity. The proposed methodology uses co-sputtering of multiple metal alloy targets in an oxygen-rich environment. Depositions are conducted at multiple substrate temperatures to identify phase transition temperatures. In addition to 100-oriented silicon, substrates composed of materials with improved lattice matching to literature values of $(MgNiCoCuZn)_{0.2}O$ are employed, and the relationship between substrate material and phase transition temperature is investigated. Various microscopic and spectroscopic characterization techniques, including Atomic Force Microscopy (AFM) and Energy Dispersive X-ray Spectroscopy (EDS), etc., were used to determine the film growth rate and stoichiometry. Molecular Dynamics simulations, with interatomic interactions provided by fine-tunned machine learning models, are employed to study the relationship between phase transition temperature and substrate composition. The computational findings for the influence of substrate composition and deposition stoichiometry on the phase transition temperature are then compared with the experimental results. The pathways for integration of the resulting film into memristive devices are also discussed.

11:00am **AM2+EM+TF-FrM-12 Electron beam lithography enabled nano EC-RAM development and fabrication**, ***Stefan Theodoru***, *Garry Rubloff,* UMD College Park*; Marshall Schroeder,* DEVCOM ARL

The exponential increase of computing demand is currently only being met with <10% improvement of computational power density per chip generation. Improvements in energy consumption have not kept pace with either industry demand or grid capacity. Electrochemical random-access memory (EC-RAM) is well postured to fulfill this demand, boasting six orders of magnitude modeled energy consumption lower than CMOS technology. EC-RAM models predict downscaling energy consumption based on micron scale devices which should at the nano scale deliver atto J cost per computation compared to the current pico J state of the art. Further boons to EC-RAM include its intrinsic non-volatility, analog states, and co-located compute and memory centers. This makes EC-RAM ideal for use in neural network computation. Scaling studies to prove these modeled results have not yet been conducted in the sub 100nm regime however, leaving a large gap between EC-RAM’s modeled capabilities, and what has been experimentally proven.

This presentation describes the process development done to fabricate Au, TiO_2, and LiPON EC-RAM devices and the results of their characterization. We use TiO_2 for its wide range of conductance states as a function of Li content. While LiPON is both well known to the research group, and provides a source of Li provided during the LiPON deposition. Process development was needed to develop sub 100nm feature separation/widths using electron beam lithography, as well as to allow for nanolithography of the reactive LiPON film (Fig.2). Devices built for performance use the vertical architecture, see Fig.1, which minimizes the ion diffusion pathway. Devices built to allow for characterization using Raman and Plume SEM use the lateral architecture, see Fig.3. Both architectures have channels defined by the width of the source/drain and their separation, and have asymmetric and symmetric variants which allow us to test the impact of having a Li reservoir on device performance. The most important parameters for defining EC-RAM performance are state change speed, retention, and cycle life of the device. State change speed is the time it takes to intercalate enough Li^+ ions into the channel that the conductivity, as read by a bias across source and drain, changes to encode a unique conductance state. Retention is defined as the time that a written state endures with no applied gate voltage. The analysis of these characterization results and process development elucidate ideal EC-RAM architecture and fabrication methodology.

11:15am **AM2+EM+TF-FrM-13 Limitations of Layered Dielectrics**, ***Peter Dickens***, *Brianna Klein, Andrew Binder,* Sandia National Laboratories, USA

Next-generation power conversion systems increasingly rely on SiC power MOSFETs to minimize switching losses and maximize power density. Conventional SiO_2 gate dielectrics limits maximizing the gate capacitance and drive current, making higher-k dielectrics attractive to improve switching characteristics.However, to date, severe defect densities at the direct high-k/SiC interface has prevented strict high-k adoption.Consequently, recent work has focused on utilizing a dielectric bilayer with SiO_2 serving as the interface dielectric with SiC to enable low defect densities and a high-k stacked on top in an attempt to gain the “best of both worlds”.Despite some reported successes, there remain critical gaps discussing what fundamental advantages or limitations exist from this dielectric bilayer approach.

In this presentation, we present analysis of the available design space for layered dielectrics in SiC-based MOSFETs.Our analysis operates under three fundamental assumptions related to applied gate bias, avoidance of time-dependent-dielectric-breakdown (TDDB), and the requirement to be high-k (effective dielectric permittivity greater than the permittivity of the

semiconductor).We show that when these assumptions are applied then the available design space for layered dielectrics is quite limited and calls into question advantages of a layered approach.

Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC (NTESS), a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration (DOE/NNSA) under contract DE-NA0003525.

SAND2026-21413A

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