Advanced Microelectronic Materials and Devices Mini-Symposium
Room 318 - Session AM2+EM+TF-WeA

Devices I

Moderators: Dr. Devika Choudhury, ASM, **Dr. Philip Lee**, University of Kentucky

3:30pm **AM2+EM+TF-WeA-6 Beyond Binary Erasure: Harnessing a Constrained RESET Operation for Analog Synaptic Plasticity in ReRAM**, ***Marius Orlowski,*** Virginia Tech

Neuromorphic computing overcomes von Neumann bottlenecks by co–locating memory and processing. Filamentary ReRAM and CBRAM are promising synaptic candidates due to compactness, non–volatility, and analog tunability, but conventional binary SET/RESET offers coarse control over conductance. This work reports a novel regime in Cu/TaO_x/Pt CBRAM—constrained RESET—where a compliance–limited RESET strengthens rather than ruptures the filament. For high–resistance filaments (R_{on} > 1 kΩ), constrained RESET reduces resistance up to tenfold, while robust filaments are unaffected, making the effect self–limiting and most useful for fragile states. The reconstruction of the Cu atom filament leads to reduced electric fields, reduced Joules heat, and reduced resistance, rendering this mechanism self-limiting. Electrostatic simulations show that a weak filament (truncated cone) concentrates electric field at its narrow tip (>1.6×10^6 V/cm) under negative bias, driving Cu^+ electromigration toward the constriction and forming a stable hourglass (double–cone) morphology. To harness this for analog weight control, we integrate the memristor with a series transistor operating in saturation, providing tunable compliance current (I_{cc}). Using pulse trains, we implement two programming techniques: (i) Incremental Step Pulse with Verify Algorithm (ISPVA), modified to stay below the rupture threshold, and (ii) Incremental Gate Voltage with Verify Algorithm (IGVVA), where gate voltage (hence I_{cc}) is incremented with fixed programming pulses. The three control parameters (ramp rate, compliance current, stop voltage) map to biological learning mechanisms, enabling precise, linear, symmetric synaptic weight updates. This work addresses three persistent challenges: instability of high–resistance states, asymmetry between potentiation/depression, and lack of linear analog control. The constrained RESET operation, implemented with transistor–based compliance control, provides stable, fine–grained weight updates. It is fully compatible with existing ReRAM stacks, adds no fabrication complexity, and improves retention and variability, accelerating commercialization for edge AI, robotics, and autonomous systems. The advantages of the new potentiation technique include: (i) Precise and stable analog resistance control for reliable synaptic weight updates, (ii) Non-destructive constrained RESET enabling symmetric and linear weight modulation, (iii) High-resistance state stabilization for improved memory retention and device reliability.

4:15pm **AM2+EM+TF-WeA-9 Epitaxial β-Ga_2O_3 Thin Films on Mica Integrated with Copper Heat-Dissipating Electrodes for High-Power Devices**, ***Ping-Hsien Wu,*** *Ying-Hao Chu,* National Tsing Hua University, Taiwan

Gallium oxide (Ga_2O_3) has recently attracted significant attention as an ultra-wide-bandgap semiconductor for next-generation high-power electronic devices. In high-power applications, device operation generally relies on high voltage and low current to reduce conduction losses. However, conventional device design faces a trade-off between reducing on-resistance and maintaining high breakdown voltage, as thinner drift layers lower resistance but also degrade voltage endurance. To address this limitation, materials with high critical electric fields are essential. Ga_2O_3 offers a significantly higher critical electric field than conventional semiconductors such as Si and SiC, enabling high breakdown voltage operation even at reduced thickness, thereby improving power efficiency. Nevertheless, its low thermal conductivity remains a critical challenge due to heat accumulation and potential thermal breakdown. In this work, high-quality Ga_2O_3 thin films with a rocking curve full width at half maximum (FWHM) of approximately 0.3° were achieved, indicating excellent crystalline quality. The Ga_2O_3 films were epitaxially grown on two-dimensional artificial mica substrates and subsequently transferred onto high-thermal-conductivity copper foils to enhance heat dissipation. In addition, a pn heterojunction composed of 600 nm-thick Ga_2O_3 and NiO was fabricated, exhibiting a breakdown voltage exceeding 500 V. The proposed structure simultaneously preserves high-voltage capability and improves thermal management, demonstrating a promising approach for high-power Ga_2O_3-based electronic devices.

4:30pm **AM2+EM+TF-WeA-10 Ultra-thin nickel films for 4H-SiC Schottky barrier diode**, ***Renato Beraldo,*** UNICAMP, Brazil

4H-SiC Schottky barrier diode (SBD) devices were fabricated on n-type 4H-SiC substrates using an ultrathin nickel film of 2 nm as the Schottky contact layer, deposited via electron-beam evaporation. First, the ohmic contact was formed using 100 nm of nickel, and the samples were annealed at 950 °C for 5 minutes. Subsequently, 2 nm of Ni was deposited, and the devices were subjected to various annealing temperatures. To create the metallic contact, 300 nm of Al was deposited by thermal evaporation and patterned into pads of 2 mm diameter without any shielding structure. The influence of annealing temperature on electrical performance and interface quality was evaluated. Electrical characteristics were measured using a parameter analyzer, and surface morphology was analyzed by atomic force microscopy (AFM). For comparison, reference SBDs with a conventional 100 nm Ni film were fabricated and characterized under identical conditions.

A set of samples was annealed at temperatures ranging from 500 to 700 °C in 50 °C steps for each sample. After the annealing treatment, the final thickness was approximately 8 nm, as measured by AFM. Electrical measurements showed that diodes were obtained at all annealing temperatures, but the best electrical performance was achieved at 650 °C, with devices annealed at 500 °C and 700 °C showing inferior rectifying behavior. For comparison, a reference Schottky diode with a 100 nm thick Ni film was fabricated. The results revealed that the 2 nm diodes exhibited a Schottky barrier height (SBH) of 1.2 eV compared to 1.6 eV for the 100 nm diodes. However, the 2 nm diodes showed a rectification ratio two orders of magnitude larger and a leakage current of 22 pA compared to 3.2 nA at -200 V. Leakage current was also measured as a function of temperature from 25 to 175 °C. From 25 °C to 50 °C, the leakage current was approximately five times lower for the 2 nm devices compared to the 100 nm devices. Finally, the density of interface states was extracted from the 2 nm device, yielding a value of $10^{12}cm^{-2}eV^{-1}$, while the 100 nm device showed values around 10^{13} $cm^{-2}eV^{-1}$.

For future analysis, devices with lateral shielding will be fabricated to compare the breakdown voltage. Additionally, HRTEM and XPS characterization will be performed to verify the silicide composition stoichiometry and the presence of undesirable carbon clusters.

4:45pm **AM2+EM+TF-WeA-11 GaN Nanoscale Vacuum-Channel Transistors**, ***Huu Nguyen,*** *George Wang, Keshab Sapkota,* Sandia National Laboratories

Field-emission-based nanoscale vacuum-channel transistors (NVCTs) can combine the robustness of vacuum devices with state-of-the-art lithography techniques enabling low operating power, on-chip integrability, energy efficiency, and high-performance stability in extreme environments such as high temperatures and high radiation. By scaling device channels to be below the electron's mean-free path in air, the NVCTs can be operate in air while maintaining the ballistic electron transport characteristic of vacuum. Here, we report experimental and modeling results of top-down fabricated, single emitter gallium nitride (GaN) lateral NVCTs. We used electron beam lithography along with dry and wet etching to fabricate GaN NVCTs with device channel lengths less than 60 nm. The devices exhibited stable high field-emission current up to 100 nA, with tuning on/off ratio greater than 10^3. Minimal leakage current from the gates was observed to be less than 0.1 nA. Finite-element (COMSOL) modeling showed strong electric field penetration of GaN emitter led to emission current modulation by the gate voltage. This study elucidates the operation of field emission based lateral gated devices and provides important understanding in the design and operation of these new class of devices. *Sandia National Laboratories is managed and operated by NTESS under DOE NNSA contract DE-NA0003525. This work was performed, in part, at the Center for Integrated Nanotechnologies, a U.S. Department of Energy, Office of Basic Energy Sciences user facility. This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.*

5:00pm **AM2+EM+TF-WeA-12 Atomic Layer Etching of Yttrium Orthovanadate Using Sequential Exposures of H_2 and SF_6/Ar Plasma**, ***Mariya Ezzy***, *Emanuel Green, Will Pajak, Andrei Faraon,* California Institute of Technology*; Joonhee Choi,* Standford University*; Austin Minnich,* California Institute of Technology

Yttrium orthovanadate (YVO) is a promising host crystal for rare-earth ion (REI)-based quantum devices, such as quantum memories and quantum transducers. The long optical lifetimes of REIs require coupling to optical resonators for faster single-photon emission and for enabling single-ion control. Such resonators are currently fabricated through focused ion beam (FIB) milling, which can leave rough, defect-rich surfaces that can degrade optical and spin properties, such as spectral diffusion. Atomic layer etching (ALE) has the potential to mitigate these fabrication-induced defects through precise, nanometer-scale etching and its surface smoothing effect. Here, we report the first ALE process for YVO in a home-built plasma etcher using an H2 plasma modification step followed by an SF6/Ar plasma removal step. Preliminary results indicate an etch rate of 0.35 Å per cycle. The etch rates, surface morphology, and surface chemical composition are characterized using atomic force microscopy and X-ray photoelectron spectroscopy (XPS).

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