Advanced Microelectronic Materials and Devices Mini-Symposium
Room 318 - Session AM1+EM+TF-WeA

Industry Perspective

Moderators: Dr. Robert Grubbs, IMEC Belgium, **Dr. Sarah Lynch**, TEL Technology Center, America, LLC, USA

2:15pm **AM1+EM+TF-WeA-1 Memory Centric AI and the Role of Advanced Materials in Future Semiconductor Technologies***, **Shivani Srivastava**,* Micron Technology **INVITED**

The rapid growth of artificial intelligence (AI) is shifting system design from compute-centric to memory-centric architectures, where bandwidth, capacity, and energy efficiency increasingly determine performance. For AI workloads, the resulting memory bottleneck is creating new demands on semiconductor materials, processes, and integration schemes.

This talk will examine how these demands are influencing the future direction of advanced DRAM, High Bandwidth Memory (HBM), 3D and emerging nonvolatile memory technologies.

In DRAM, continued scalingis increasingly associated with efforts toward leakage reductions, variability minimization, and the exploration of novel integration schemes to optimize performance.

In parallel, industry trends toward increasing 3D DRAM layer counts are driving the need for high aspect-ratio etch and gap fill, conformal deposition, and high-quality epitaxial growth approaches.

While HBM, advanced CMOS integration, and heterogeneous packaging are becoming essential to reducing the compute-memory gap, thermal-mechanical reliability, power efficiency, and co-packaged optics are expected to play an increasing role in improving system-level performance.

Across these platforms, thin-film process control, conformality, interfaces, defect management, thermal-mechanical reliability, and system-level co-optimization are emerging as central levers for overcoming the AI memory wall.

2:45pm **AM1+EM+TF-WeA-3 Angstrom-Era Logic: From Nanosheets to Hybrid Bonding***, **Biswajeet Guha**,* Intel Corporation **INVITED**

Advanced microelectronics scaling has entered an era in which performance and density gains can no longer come from transistor miniaturization alone. Innovation now spans two tightly coupled fronts—front-end device architecture and advanced heterogeneous packaging—unified under the emerging paradigm of System Technology Co-Optimization (STCO). This talk presents a material-centric perspective on both, highlighting opportunities for the AVS community to contribute foundational research.

At the transistor level, the transition from FinFET to gate-all-around (GAA) nanosheet architectures, exemplified by angstrom-class nodes such as 18A, restores electrostatic control while introducing demanding materials challenges in high-k interfaces, work-function metals, and inner-spacers. Backside power delivery further reshapes the device stack, imposing new requirements on wafer thinning, through-silicon contacts, and thermal management, while contact and interconnect resistance remain critical bottlenecks demanding novel liner/barrier schemes and interface engineering.

Equally consequential are the materials challenges in advanced packaging, where scaling has shifted to the system level through heterogeneous integration. Fine-pitch hybrid bonding makes void-free Cu–Cu and dielectric–dielectric joining a surface-science problem governed by oxidation control, CMP dishing, and surface activation. Stacked high-power dies intensify the need for advanced thermal interface materials and careful management of CTE mismatch, while fine-line redistribution layers, low-loss dielectrics, underfills, and interposers each present challenges in adhesion, stress, and warpage.

By framing transistor and packaging innovation together through an STCO lens, this talk argues that the future of microelectronics depends on co-optimizing materials, processes, and architectures across the entire system—offering fertile ground for the surface- and materials-science community.

3:15pm **AM1+EM+TF-WeA-5 Epitaxial CVD Ruthenium for High-Performance Interconnects at A7 and Beyond***, **Gyana Pattanaik**,* Tokyo Electron America

Ruthenium is projected to replace Cu in A7 node or beyond, likely bringing back subtractive integration that Cu replaced with damascene almost 3 decades ago. To enable this transition, integration of Ru interconnect metal lines and vias with lower resistivity need to be demonstrated. Ru thin films with very low resistivity (~8 μΩ-cm at 30nm; bulk =7.4 μΩ-cm) has been reported [1], by depositing epitaxial PVD Ru on Si (111) with buffer layers like AlN (001). Layer transfer approach has been proposed for integration of such epitaxial Ru [1]. PVD epi-Ru can be suitable for interconnect metal lines through patterning and direct metal etch. However, it may not be ideal for via, even though some integration approaches explore to use it. CVD via filling remains an attractive integration approach for via metal [2]. Here we demonstrate epitaxial CVD Ru for selective via filling (Fig 1).

In this study, we used epitaxial PVD Ru (6 and 8 nm)/AlN (001)/Si(111) as substrates for CVD Ru experiments conducted in a CVD reactor. A series of preclean steps was applied to eliminate surface oxides and refresh the surface before CVD Ru growth under different deposition conditions. Powder XRD patterns (2θ-ω scans) show only Ru (*00l*) peaks, indicating CVD Ru film growth along *c*-axis. Representative CVD Ru film growth is shown in Fig 2. Laue oscillations at the bottom of Ru (002) peak are signature of epitaxial film growth. The Ru (101) Φ-scans collected at c=61.3^{0} show six-fold symmetry (Fig 3), like the underlying PVD epi-Ru, further confirming epitaxial CVD Ru film growth [1]. This paper will summarize systematic studies of CVD Ru film growth on PVD epi-Ru and characterizations including microstructure and electrical properties.

References:

1. C. Adelmann et.al, Epitaxial Ruthenium for Advanced Interconnects, IITC (2025) P32.
2. M. H. van der Veen, et. al, Selective Deposition and Ruthenium Superfill Exploration Beyond A10 Node Interconnects, VLSI Symposium (2025), T18-3.

Keywords: Interconnects, Ruthenium, Epitaxy, CVD

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