Plasma Science and Technology
Room 315 - Session PS2+EUV-TuA

Plasma Processes for Feature Scaling

Moderators: Prof. Dr. Erwin Kessels, Eindhoven University of Technology, the Netherlands, **Dr. Pingshan Luan**, TEL Technology Center America

4:00pm **PS2+EUV-TuA-8 Advanced Logic Pitch Scaling in the High NA EUV Era***, Arame Thiam,* ***Yannick Feurprier,*** TEL Europe, Belgium **INVITED**

High NA (0.55 NA) EUV lithography enables the single exposure of critical layers for future generations of logic (14A and below) and DRAM (1d and below) devices. Its implementation, however, introduces challenges in meeting both technology and high-volume manufacturing requirements. We will review and discuss the challenges of certain processes for logic use cases (Place and Route and Tip-to-Tip CD control, random logic via) and for the memory cases (contact holes and pillar). Co-optimization of the lithography process (resist, source, mask and development method) together with the etch pattern transfer process and the defectivity assessment enables the demonstration of a failure free process window for Place and Route (PnR) logic clips at tight pitches (down to 18 nm pitch) and for 28 nm pitch pillars for the memory use case.

The stringent tip-to-tip (T2T) CD control required by the technology in the PnR also creates opportunities for directional etch techniques. Gas Cluster Beam (GCB) technology can complement high NA EUV lithography by providing precise T2T CD control, reducing LER and helping to mitigate defectivity. Finally, further validation of the high NA EUV and etch patterning transfer is presented through electrical test.

Keywords: High NA EUV, Etch patterning, PnR, DRAM, Defectivity, Directional etch, Electrical test

4:30pm **PS2+EUV-TuA-10 Dry Resist Patterning Solutions for High-NA EUV Lithography***, Ali Haider,* Lam Research Corp.*; Zhengtao Chen, Shruti Jambaldinni,* Lam Research Belgium BV, Belgium*; Anuja De Silva,* Lam Research*; Rich Wise,* Lam Research Corp. **INVITED**

High-NA EUV lithography patterning at increasingly tight pitches introduces significant challenges, including elevated defectivity, reduced depth of focus (DOF), shrinking process windows, and the need for dose reduction without degrading pattern quality. These challenges become increasingly severe near ultimate resolution at P18 L/S and limit the extendibility of conventional wet solution processed resists.

In this work, we demonstrate the performance of Lam's Aether® dry resist technology for dense P18 line/space patterning using high-NA EUV lithography. We address key challenges such as defectivity, DOF, and line wiggling through co-optimization of dry resist deposition, underlayer, post exposure bake (PEB), and dry development. We introduce next-generation dry resists based on novel precursor chemistries with enhanced EUV sensitivity, enabling reduced dose to size without compromising roughness, while expanding the defect-free process window through co-optimization with dry development. We further introduce new dry development schemes that increase the effective resist budget after development, resulting in improved defect performance and lower roughness.

To address the high NA EUV challenge of limited DOF and profile control, we have introduced 3D engineered dry resist films using multi layer deposition with controlled composition and tunable EUV sensitivity in the vertical direction.1,2 We show that 3D engineered resist provides lower dose to size, improved profile control, reduced line wiggling, and enhanced DOF.

Overall, we show that Aether dry resist and development solutions address key challenges in high-NA EUV P18 L/S through innovations in dry resist and development strategies with co optimization of process parameters.

[1]Gulati, Saumya, et al. "Evaluating three dimensionally engineered dry resist film performance for 0.33 NA and High-NA EUV patterning." Advances in Patterning Materials and Processes XLIII. Vol. 13983. SPIE, 2026.

[2]A. Haider et al., "Advances of dry resist towards next-generation lines-spaces patterning in high-NA EUV lithography," Proc. SPIE 13686, 1368608 (2025)

5:00pm **PS2+EUV-TuA-12 Study of Electron-Induced Etching Mechanisms for Chromium and Ruthenium** *, **Michael Hinshelwood**, Gottlieb S. Oehrlein,* University of Maryland, College Park*; Hubertus Marbach, Michael Remmel, Gerson Mette, Michael Budach, Daniel Rhinow, Klaus Edinger, Maik Szafarska,* Carl Zeiss SMT GmbH, Germany

Chromium (Cr) and ruthenium (Ru) are materials critical for semiconductor manufacturing, particularly as part of DUV and EUV photomasks, respectively. Both can be effectively etched with plasmas containing both oxygen and a halogen. Cr can be etched through the formation of CrO_2Cl_2 or CrO_2F_2, while Ru is etched through the formation of RuO_4 or volatile RuO_xCl_y. To limit surface damage caused by ion bombardment during plasma etching, there is significant interest in isolating ions from the reaction system.

Y. Li et al. demonstrated rapid etching of Ru by combining a low-energy electron beam (EB) with a remote plasma (RP)-created flux of O_2/Cl_2-derived neutrals [1]. The combination of EB and RP resulted in a synergistic etch effect, while RP or EB alone caused either low-rate etching or growth. Here, we aim to describe the mechanism that leads to this synergistic effect and expand it to the etching of Cr, and also investigate how etching selectivity between the two materials may be achieved.

Using in-situ ellipsometry, we model the real-time etching and modification of the metal surfaces. This modelling is complemented by direct chemical characterization of the surface with X-ray photoelectron spectroscopy (XPS). In the case of Ru, we have found that the EB increases the uptake of Cl on the Ru surface, which in turn activates the Ru toward oxidation to volatile compounds. The growth rate and composition of this chlorinated layer formed by the EB are investigated via XPS measurements with increasing EB/Cl_2 exposure time. In the case of Cr, we find a stronger synergistic effect with F/O etch chemistry as opposed to Cl/O. The etch rate with RP alone is highly dependent on the oxygen percentage in the feed gas as well as the oxidation state of the Cr. With a fluorine-rich feed gas, the surface quickly forms a CrF_x passivation layer, preventing further etching. The EB can break through this passivation and continue the Cr etch process by forming vacancies that allow O radicals to diffuse into the surface and form volatile Cr–O–F compounds. By combining ellipsometric observations with chemical quantification from XPS, we obtained mechanistic insight for the development of low-damage etch processes for Cr and Ru, and insights on paths to high Cr hard mask and Ru capping layer selectivity.

[1] Y. Li *et al.*, "Investigation of ruthenium etching induced by electron beam irradiation and O_2/Cl_2 remote plasma-based neutral fluxes: Mechanistic insights and etching model," *J. Vac. Sci. Technol. A*, vol. 43, no. 2, p. 023005, Feb. 2025, doi: 10.1116/6.0004219.

5:15pm **PS2+EUV-TuA-13 3 Layers Dielectric Patterning in Grid Module for OSC 3DDRAM Application***, **Yuchao Jiang**, Jeongsoo Kim, Alejandro Fernandez Rodriguez, Hemant Kumar Raut, Nouredine Rassoul, Eren Canga, Robert Carpenter, Attilio Belmonte, Katia Devriendt,* IMEC, Belgium

3 layers dielectric patterning in Grid module for OSC 3DDRAM application

Yuchao. Jiang[1], Jeongsoo Kim[1], Alejandro Fernandez Rodriguez[1], Hemant Kumar Raut[1], Nouredine Rassoul[1], Eren Canga[1], Robert Carpenter[1], Attilio Belmonte[1] and Katia Devriendt[1]

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DRAM applications have reached a limiting point with 2D design (planar device) because of the process challenges for ~12nm nodes and scaling difficulty of density. Since 2011, monolithic 3DDRAM has been explored with different integration approaches (HBL, VBL, capacitorless etc), and recently it has experienced renewed interest by major players in memory market.

In this presentation, a dry–etch process for grid patterning in MOLD–based monolithic 3D DRAM was reported, the process enables robust isolation of active regions in vertical–bit–line architectures. The method addresses morphology degradation and sidewall profile asymmetry arising from pattern–loading effects and hard–mask facet evolution in multi–layer SiN/SiO_2 ONO stacks. By optimizing passivation balance, ion directionality, and process conditions, the approach achieves stable dielectric grid formation with controlled critical dimensions and near–vertical sidewalls. The demonstrated process provides reproducible grid patterning suitable for high–aspect–ratio 3D DRAM integrationIn monolithic 3DDRAM with MOLD–based vertical–bit–line (VBL) architecture, the Grid module (SINGRID) is the key dielectric–etch step that isolates active areas by etching through a multi–layer SiN/SiO_2 ONO structure (~355 nm). The grid lines have tight CD requirements and require near–vertical profiles (>87°) to ensure VBL alignment and prevent capacitor/gate shorts.

The grid exhibits major–axis vs. minor–axis HM (hard–mask) facet differences, caused by imbalanced ion/radical flux between dense vs. semi–dense regions. Consequences include:

1. Unequal CD narrowing
1. Facet tilt differences (leading to asymmetric top rounding)
2. Risk of local bowing when ARDE.

For morphology improvements, a leaner DARC open step is applied (with reduced CHF3 and increased CF4/O2 flow) to reduce the morphological deformation.

For sidewall profile improvements, the process mitigates these effects through controlled anisotropic dry etching, combining directional ion bombardment with carefully tuned sidewall passivation.

5:30pm **PS2+EUV-TuA-14 Role of Interfacial Force Balance in Gap Filling of TEOS-based Flowable CVD: Insights from Molecular Dynamics***, **Hu Li**,* Tokyo Electron America Inc.,*; Takeo Nakano, Nobuo Matsuki, Masaaki Matsukuma,* Tokyo Electron Ltd., Japan*; Raymond Joe, Anthony Dip,* Tokyo Electron America Inc.,

Achieving void-free gap filling in high-aspect-ratio structures is one of the key challenges in advanced semiconductor processing. Flowable chemical vapor deposition (CVD) has been widely studied as a promising approach, and its behavior is often interpreted in terms of wettability or viscosity. However, these conventional descriptors do not always explain the differences observed in gap-fill performance across various precursor chemistries and geometries.

In this work, we focus on the pre-cure stage of flowable CVD and investigate the transport-driven filling behavior using classical molecular dynamics simulations. By intentionally excluding chemical reactions, we isolate the role of intermolecular interactions and interfacial forces in confined geometries. The simulation system consists of siloxane-based liquids on SiO_2 substrates, with trench structures of varying aspect ratios.

To better understand the filling mechanism, we introduce a force-based analysis by decomposing the total force acting on liquid molecules into liquid-substrate and liquid-liquid contributions. This approach reveals a clear spatial variation in the driving forces within the trench. Near the sidewall, strong downward forces promote infiltration, while in the center region, the driving force is significantly reduced, which leads to incomplete filling and void formation.

We further show that increasing the aspect ratio enhances this imbalance in force distribution, making uniform filling more difficult. In addition, surface modification, such as Si-rich surface, can reduce the interfacial interaction strength and improve liquid mobility.

These results suggest that gap-fill behavior cannot be fully described by wettability alone, and that a force-based perspective provides more direct insight into the underlying mechanism. This study offers a more detailed understanding of pre-cure transport processes and may help guide the design of future flowable CVD processes.

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