## Advanced Microelectronic Materials and Devices Mini-Symposium

## Room Ballroom A - Session AM+EM+TF-ThP

## Advanced Microelectronic Materials and Devices Mini-Symposium Poster Session

**AM+EM+TF-ThP-1 AlScN Ferroelectric Diode-based Non-volatile Memory on $TaSi_2$ for Harsh-Environment Computing**, ***Nghi Pham,*** University of Pennsylvania, Viet Nam; *Dhiren Pradhan,* Agni Semiconductor; *Xindi Yang, Ravali Gudavalli, Deep Jariwala,* University of Pennsylvania

Electronic systems capable of operating in harsh environments—including space exploration (e.g., Venus and near-solar probes), aeronautics, oil and gas exploration, nuclear power plants, and heavy industrial processes—must withstand extreme temperatures and radiation. These applications demand in situ computing and sensing with stable performance under extreme conditions. However, no NVM technologies reliably function above 250 °C, creating a critical gap in high-temperature electronics. Despite well-established high-temperature logic with reliable operation > 800 °C, the absence of a compatible NVM technology hinders fully integrated computing for extreme environments. Ferroelectric diodes (FeDs) are promising candidates for selector-free, non-volatile memory (NVM) due to their nonlinear current–voltage behavior, potential multistate operation, and simple two-terminal architecture. For harsh-environment electronics, however, maintaining a high ON/OFF ratio and stable switching at elevated temperatures remains a major challenge, largely due to stronger internal fields and increased charge trapping.

In this work, we have successfully grown 45 nm of $Al_{0.68}Sc_{0.32}N$ on $TaSi_2$ despite the large lattice mismatch. $TaSi_2$ is a well-known high-temperature metal electrode and has been employed in NASA's Junction Field Effect Transistors (JFETs). The XRD omega scan of $Al_{0.64}Sc_{0.36}N$ reveals a full width at half maximum (FWHM) of 4.06°. Stacks with and without an $AlO_x$ interlayer were compared to evaluate the role of interfacial engineering in leakage suppression, switching behavior, and ON/OFF ratio retention at elevated temperatures. The devices consisted of Ni top electrodes, a ~10 nm $AlO_x$ interlayer (IL) dielectric, a ~45 nm AlScN ferroelectric layer, and $TaSi_2$ bottom electrodes.

Temperature-dependent DC-IV, AC-IV, and Positive-Up Negative-Down (PUND) measurements were performed up to 800 °C. For the 32% Sc AlScN device without an IL dielectric, the ON/OFF ratio remained measurable, decreasing from ~10 at 25 °C to 2.37 at 800 °C. By contrast, devices with an $AlO_x$ IL dielectric exhibited substantially higher ON/OFF ratios, reaching values above 500 at room temperature and ~6 at 800 °C. These results highlight the role of $AlO_x$ interfacial engineering in suppressing leakage and improving state distinguishability at elevated temperatures. High-temperature ferroelectric polarization switching, and other NVM characteristics such as read and write endurance, retention measurements of the ferrodiodes of $Al_{0.68}Sc_{0.32}N$ on $TaSi_2$ with 10 nm $AlO_x$ IL dielectrics up to 900 °C are currently underway and will be presented at the meeting.

**AM+EM+TF-ThP-2 Flexible Ag and Cu Pattern Films: A Comparative Study on Conductivity, Adhesion, and Mechanical Stability**, ***Seonhee Jang,*** *Samuel Goutierrez, Kenneth Lathrum,* University of Louisiana

The integration of metallic nanoparticles (NPs) has revolutionized the fabrication of flexible electronic devices. Compared to their bulk counterparts, metallic NPs exhibit unique shape and size-dependent properties that make them indispensable to the electronics industry. However, achieving superior electrical conductivity requires specialized post-processing to remove the stabilizing agents and additives used during NP synthesis.

In this study, silver (Ag) and copper (Cu) NP inks were employed to fabricate conductive patterns via printing and sintering processes for flexible electronics applications. These inks were printed onto 0.1 mm thick flexible Kapton polyimide (PI) sheets. The Ag ink was formulated with a solid content of 42±2 wt%, a density of 1.6 g $mL^{-1}$, and a viscosity of 3.5-6.0 Pa S at 10 $s^{-1}$. The Cu NP ink featured a solid content of 88 wt%, a density of 3.9 g $mL^{-1}$, and a viscosity of 20-40 Pa S at 50 $s^{-1}$.

Metal NP patterns were printed using a single-nozzle printing system and subsequently dried and sintered under four distinct sintering conditions: thermal treatment only (TO), laser irradiation only (LO), thermal treatment followed by laser irradiation (TL), and laser irradiation followed by thermal treatment (LT). This allowed for a comprehensive comparison of single and dual sintering techniques on the physical, chemical, mechanical, and electrical properties of the metal patterns. Post-sintering evaluations include microstructure analysis, crystallography, chemical composition, electrical sheet resistance, and mechanical strength.

The results demonstrated that for Ag patterns, the LT condition yielded the best performance for flexible electronics, achieving the lowest sheet resistance (0.0031 Ω $Sq^{-1}$) and superior mechanical stability ($R/R_0$=1.75) due to enhanced grain growth and effective organic removal. For Cu patterns, the TO condition proved optimal; while the LT condition provided the lowest resistance (0,0117 Ω $Sq^{-1}$), the TO condition ensured more uniform grain growth and higher flexibility ($R/R_0$=10.58). Overall, Ag patterns outperformed Cu in both conductivity and adhesion, as Cu suffered from oxidation and brittleness associated with high hardness (37.18-55.36 $N/mm^2$). These findings suggest that optimizing sintering parameters such as laser intensity and thermal atmosphere can further enhance the overall properties of Cu. Moreover, the adoption of dual sintering methods can improve the performance of printed flexible electronic devices, and there are more scopes for continuing research related to this method.

**AM+EM+TF-ThP-3 Study of Acoustoelectric Interactions in α-$In_2Se_3$ - $LiNbO_3$ Heterostructure for Efficient RF Communication System**, ***Marzia Sultana,*** *Jackson Anderson,* University of Vermont

The growing global demand for energy is creating an urgent need for more efficient computation and communication technologies (Figure 1a) [1]. Despite vast improvements in computational efficiency, modern radio systems integrated on-chip still cannot simultaneously transmit and receive data (Figure 1b). Although circulators enable concurrent transmission and reception, conventional designs rely on magnetic fields, making them difficult to integrate with modern semiconductor technologies (Figure 1c) [2]. Acoustoelectric devices provide a promising magnet-free alternative for realizing compact and energy efficient circulators. In this work, we explore a novel heterostructure based on α-$In_2Se_3$ which is a two-dimensional ferroelectric semiconductor with moderate bandgap (1.39 eV) and carrier mobility up to 3392 cm2/(V*s) [3]. This study will be carried out in three main stages. The first stage focuses on simulating the acoustoelectric device gain to optimize heterostructure dimensions based on key material properties of α-$In_2Se_3$, such as carrier mobility and doping concentration. The second stage involves 2D material fabrication through mechanical exfoliation and characterization of exfoliated α-$In_2Se_3$ flakes to evaluate practically achievable device performance (Figure 2). In the final stage, the optimized structure will be integrated into a complete device design guided by simulation results. The simulation framework for the α-$In_2Se_3$–$LiNbO_3$ heterostructure was first validated against an existing InGaAs–AlScN design [4]. The proposed model exhibits higher gain in the low-frequency regime (Figure 3a). Additionally, the gain-to-power ratio (Figure 3b) indicates improved efficiency, attributed to the moderate carrier mobility of α-$In_2Se_3$. While higher mobility (InGaAs) can increase gain, it also leads to greater power dissipation, reducing overall efficiency. Figure 4 illustrates the impact of doping concentration on performance. Maximum gain is observed near a doping level of $10^{16}$ $cm^{-3}$ (Figure 4a), whereas efficiency is higher at lower doping levels (Figure 4b). An optimal operating region is identified (Figure 4c), where both gain and efficiency are balanced. At 1 GHz, the device achieves a gain of 37.8 dB with a low power dissipation of only 0.02 mW. Mechanical exfoliation of α-$In_2Se_3$ using different adhesives initially produced poor-quality flakes, prompting investigation of process parameters such as substrate baking conditions. Increasing the baking temperature from 150°C to 200°C improved flake uniformity and size, and a Design of Experiments approach will be used to further optimize yield for device fabrication.

**AM+EM+TF-ThP-4 Spatial Mapping of Spin Wave Dynamics in Shape-Optimized Magnetostatic Wave Cavity Filters**, ***Kelsey Collins,*** Air Force Research Laboratory

Yttrium iron garnet (YIG) magnetostatic wave (MSW) radio frequency (RF) cavity filters offer wide frequency tunability, making them highly promising for sixth-generation (6G) communication systems. However, finite cavity dimensions generate severe spurious modes that degrade filter performance. While tailoring the transducing electrode shape can suppress these undesired modes and enhance the primary passband, the underlying wave dynamics remain poorly understood. This study utilizes micro-focused Brillouin light scattering (BLS) spectroscopy to spatially map and analyze the excited spin waves within the cavity. Spatial profiles reveal that conventional straight-line electrodes exhibit frequency-dependent mode propagation. Conversely, optimized half-cone electrodes maintain consistent spin wave propagation across the entire frequency range. These findings demonstrate that electrode shaping directly controls the RF passband by stabilizing constituent spin wave propagation, offering critical insights for designing high-performance, spur-free nonreciprocal devices.

**AM+EM+TF-ThP-5 Nanoscale structural and chemical characterization of AlxTi1-xN wurtzite thin films.***, **Sai Saswat Tripathy**, Elizabeth Dickey,* Carnegie Mellon University*; Ian Mercer, Jon-Paul Maria,* Penn State University

Wurtzite ferroelectrics based on the composition $Al_{1-x}M_xN$, with M representing transition metals, have shown to possess large remnant polarization values, and higher thermal stability than conventional ferroelectrics like lead zirconate titanate (PZT) or barium titanate (BTO), and thus find potential applications in high operating temperature non-volatile memories. In this study, transmission electron microscopy (TEM) and scanning transmission electron microscopy-based energy-dispersive X-ray spectroscopy (STEM-EDS) were employed to investigate the structural and chemical characteristics of a stack comprising of a silicon substrate, titanium bottom electrode with a thin TiN layer, $Al_{0.92}Ti_{0.08}N$ thin film and tungsten top electrode. $Al_{1-x}Ti_xN$ based wurtzite thin films have previously been used for piezoelectric applications, and have potential ferroelectric applications, if polarization switching by the application of external electric field can be shown. Electron-transparent cross-section lamellae were prepared from the stack using focused ion beam (FIB) milling to enable site-specific TEM/STEM analysis. Bright-field (BF) and dark-field (DF) TEM images revealed a fiber-texture in the film with columnar grains aligned parallel to the growth direction. Zone-axis diffraction patterns (ZADPs) acquired from the film demonstrated wurtzite phase purity and c-axis oriented growth of the film. STEM-EDS revealed uniform distribution of Al, Ti and N throughout the film, further confirming wurtzite phase purity, which is essential for ferroelectric switchability.

**AM+EM+TF-ThP-6 IGZO Thermal ALD application in 3D High Aspect Ratio (HAR) Features: Conformality and Elemental Uniformity Studies***, **Adarsh Rajashekhar**, Fei Zhou,* Sandisk Technologies*; Ritwik Bhatia, Ganesh Sundaram,* Veeco Instruments*; Senaka Kanakamedala,* Sandisk Technologies

Multi-component oxide IGZO ($In_xGa_yZn_zO_p$) has been proposed as the channel material enabling low-cost and scalable future 3D-DRAM technology [1], [2]. This application would necessitate uniform deposition in high pattern density, high aspect ratio (HAR) structures. However, benchmarking of conformality and compositional uniformity in HAR structures is lacking in literature. With this objective, IGZO ALD deposition has been studied within deep hole features with two different aspect ratios (7:1 and 90:1). As a first step, a baseline deposition recipe was developed on blanket substrates. TMIn, TMGa and DEZ precursors were chosen due to their relatively high vapor pressures and well understood ALD processes. An optimal 200˚C deposition temperature avoids decomposition of DEZ and TMIn above 250˚C, while overcoming low growth-rates of $GaO_x$ below 200˚C. Precursors and Reactant ($O_3$) dose times were separately optimized to ensure growth saturation, with $GaO_x$ growth typically needing ~20x the $O_3$ dose time to ensure complete reaction, as compared to $InO_x$, $ZnO_x$. Based on these optimizations, carbon content in the developed IGZO films were found to be below the detection limit of X-ray photoelectron spectroscopy (XPS). The initial blanket baseline recipe (not optimized for HAR depositions) comprising of In-O-Ga-O-Zn-O growth sub-cycles yielded 50% coverage (bottom/top sidewall) for a 7:1 HAR structure, and 25% coverage for the 90:1 case. Specifically, In (precursor with highest molecular weight and lowest vapor pressure) saw a 21% to 38% reduction in partial fraction from top to bottom, whereas was partially compensated by Ga and Zn partial fractions increase that ranged around -3% to 20% in the different structures. Continuous coverage and compositional uniformity improvements are planned, with longer dose times as one of the knobs (and with particular emphasis on the In component).

1. D. Ha et al, "Exploring Innovative IGZO-channel based DRAM Cell Architectures and Key Technologies for Sub-10nm Node," pp 1-4 IMW (2024)

2. M. Okajima et al, "Highly stackable Oxide-semiconductor Channel Transistor Technology for Future High-density and Low-power 3D DRAM," pp 1-4 IEDM (2025)

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