CHIPS Act : Semiconductor Manufacturing Science and Technologies

Room 207 A W - Session CPS+MS-MoM

Digital Twins and Advanced Packaging for Semiconductor Manufacturing

Moderators: Tina Kaarsberg, U.S. Department of Energy, Advanced Manufacturing Office, **John Lannon**, Micross

9:00am **CPS+MS-MoM-4 An Overview of Advanced Semiconductor Packaging Activities at Arizona State University***, **Christopher Bailey**, Hongbin Yu,* Arizona State University

Arizona State University (ASU) is engaging in all aspects of the chips act including R&D as well as Education and Workforce Development (EWD) activities. At our MacroTechnology Works (MTW) facility, which is a refurbished Motorola Fab, we are installing a 300mm Fan Out Wafer Level Packaging (FOWLP) pilot line based on the DECA M-Series process flow. In addition to this, investments in metrology, EDA, and Multi-Physics modelling have been made to support innovation for future heterogeneous integrated systems.

During this presentation, I will provide an overview of advanced packaging activities underway at ASU which includes projects in the Microelectronics Commons SWAP-Hub program as well as the NAPMP SHIELD-USA project that is pushing the envelop for fan-out wafer level packaging for new substrate technologies with an aim to achieve 0.5um line/spacing and bump pitches as low as 2um. In addition to this, the presentation will detail education and workforce development programs for advanced semiconductor packaging.

9:15am **CPS+MS-MoM-5 Overview of research at the Center for Heterogeneous Integration Research in Packaging (CHIRP) Center***, **Srikanth Rangarajan**,* Binghamton University **INVITED**

The Center for Heterogeneous Integration Research in Packaging (CHIRP) is a leading research center dedicated to advancing the field of heterogeneous integration (HI) for next-generation electronic systems. This talk provides an overview of CHIRP's research activities, focusing on novel packaging technologies, materials, and designs that enable the integration of diverse components with enhanced performance and functionality. We will highlight key projects and recent advancements in areas such as chiplet-based integration, 2.5D/3D packaging, thermal management, and reliability. Furthermore, the presentation will outline CHIRP's collaborative ecosystem and its role in shaping the future of microelectronics through innovative HI solutions.

9:45am **CPS+MS-MoM-7 Re-Shoring Advanced Packaging Capabilities in a Secure Environment***, **John M. Lannon Jr**, Rex Anderson,* Micross Advanced Interconnect Technology

The CHIPS Act has garnered a lot of attention for the re-shoring (or on-shoring) of semiconductor device manufacturing, which includes device manufacturing and downstream packaging, assembly, and test of the devices. Prior to the CHIPS Act, the DoD had been developing its own initiative to de-risk mission critical microelectronics supply chain needs, the Reshore Ecosystem for Secure Heterogeneous Advanced Packaged Electronics (RESHAPE) program. The goal of this program is to ensure the defense industrial base (DIB) has access to a secure, domestic advanced packaging, assembly, and test capability. Initial awards for the program were made late in 2023 for four technical elements: 300mm wafer bumping and 300mm wafer preparation at Micross Advanced Interconnect Technology (a post-CMOS wafer processing facility in North Carolina); Fan-out Wafer-Level Packaging (FOWLP) at the SkyWater facility in Kissimmee, Florida; and Si interposer technology through BRIDG/SkyWater collaboration at the SkyWater facility in Kissimmee, Florida. In this paper, we will provide a brief overview of the RESHAPE program, then focus on the Secure Center for Advanced Packaging Excellence (SCAPEx) project awarded to Micross, covering both current capabilities and future advanced packaging capabilities coming online over the next 12 months.

10:00am **CPS+MS-MoM-8 ML-based Co-design of TSV and TGV Interposers for Advanced Packages***, Pouria Zaghari, Sourish Sinha, **Douglas Hopkins**, Jong Ryu,* North Carolina State University

Copper-filled vias are essential elements in advanced 2.5D and 3D electronic packaging, facilitating reduced form factors and enhanced system performance. This study presents a numerical parametric investigation and a machine learning–driven optimization of through-silicon vias (TSVs) and through-glass vias (TGVs). The optimization targeted three primary performance metrics: copper protrusion, thermal resistance, and electrical parasitics. The coupled influences of aspect ratio (AR) and via pitch were systematically evaluated for both square and hexagonal via array configurations.

The parametric results indicate that glass substrates outperform silicon in mitigating copper protrusion (by up to 47.5%) and reducing mutual capacitance (by up to 67.6%), while TSVs exhibit superior thermal conductivity. A high AR was associated with reduced copper protrusion, whereas low pitch and hexagonal arrays enhanced thermal performance. Conversely, high pitch and low AR configurations were more effective in minimizing electrical parasitics.

For optimization, a conventional genetic algorithm (GA) was benchmarked against a novel online artificial neural network (ANN)–based approach. The ANN method achieved a 61.3% reduction in computational time relative to the GA, underscoring its suitability for high-fidelity optimization of complex electronic packaging designs.

This framework has significant potential for integration into a digital twin environment, wherein a real-time virtual replica of an electronic package can accurately reproduce its electrical, thermal, and mechanical behavior. The computational efficiency of the ANN-based approach enables rapid, high-resolution simulations necessary for real-time digital twin applications—capabilities that are impractical using traditional GA-based optimization due to prohibitive computational demands.

The significance of this work lies in its multidisciplinary co-design methodology, simultaneously accounting for electrical, thermal, and mechanical performance metrics. By leveraging a computationally efficient ANN-based optimization, the framework offers a scalable pathway toward adaptive, self-correcting electronic systems, where digital twins can be employed to predict, monitor, and proactively mitigate potential reliability risks.

10:30am **CPS+MS-MoM-10 Digital Twins and the SRC MAPT2 Chapter on Digital Twins and Applications***, **Robert Baseman**,* IBM Research Division, T.J. Watson Research Center **INVITED**

The semiconductor industry anticipates substantial reductions in manufacturing costs and product times to market as a result of deploying digital twins throughout the design and production ecosystem.Recognizing this, the SMART USA Institute was established as part of the CHIPS Act to accelerate efforts to develop, validate, and use digital twins to improve domestic semiconductor design, manufacturing, advanced packaging, assembly, and test processes.

Here we summarize Chapter 12 of the Semiconductor Research Corporation’s Microelectronics and Advanced Packaging Technologies Roadmap2 (SRC MAPT2), a collaborative effort of experts from academia, industry, and national labs.This new Chapter in MAPT2 is intended to provide a digital twin focus to the industry Roadmap, to inform the SMART USA Institute strategy and to illustrate how digital twins will support the US NSTC Strategic Plan and the National Strategy on Microelectronics Research.

Digital twins of relevance to the semiconductor industry and considered in the Chapter include twins of a vast scope: from twins of atomic scale surface chemistry processes with a characteristic time scale of picoseconds to twins of global supply chains with a characteristic timescale of years.

The Chapter characterizes the state of the art, future industry requirements, challenges to be overcome, and enabling technical directions for twins *per se,* infrastructure enabling development & deployment of twins, and applications of twins.The Chapter includes some perspectives on assessing the impact of twin deployment and concludes with some illustrations of how digital twins will support several domestic strategic initiatives.

11:00am **CPS+MS-MoM-12 Digital Twins Meet Materials Science: Real-Time AI Analysis for Advanced Manufacturing***, **Jeff Terry**,* Illinois Institute of Technology

We have developed an artificial intelligence (AI)-driven methodology for the automated and reliable analysis of advanced materials characterization measurements, including Extended X-ray Absorption Fine Structure (EXAFS), Nanoindentation, X-ray Emission Spectroscopy (XES), and X-ray Photoelectron Spectroscopy (XPS). These techniques are critical for probing

the chemical, structural, and mechanical properties of materials at the nanoscale and are commonly deployed across semiconductor fabrication lines for quality assurance, process control, and failure analysis.

At the heart of our approach is a genetic algorithm capable of extracting physically meaningful structural parameters by fitting experimental spectra to a curated set of candidate chemical configurations. Analysts provide a preliminary list of potential compounds and corresponding computational inputs, after which the algorithm iteratively refines the model to best match the observed data. This process is implemented in our open-source Python analysis framework, **Neo**, which is designed to support modular, high-throughput, and reproducible analysis pipelines.

Importantly, Neo interfaces directly with the **XPS Oasis** and **XES Oasis** databases—comprehensive, structured repositories of curated spectral reference data. These databases allow Neo to draw from a rich library of previously characterized materials and electronic structures, significantly enhancing its ability to identify subtle differences in chemical states and bonding environments. This capability is especially valuable in semiconductor production, where minor variations in composition or surface chemistry can have outsized impacts on device performance and reliability.

By embedding this AI-enabled analysis tool within production environments, manufacturers can achieve **real-time, in-line monitoring** of materials during fabrication. Moreover, by streaming these insights into **digital twin platforms**, facilities can build continuously updated virtual models of the physical production line. These models enable predictive analytics, fault detection, process optimization, and adaptive control—ultimately reducing downtime, improving yield, and enhancing materials traceability throughout the supply chain.

CHIPS Act : Semiconductor Manufacturing Science and Technologies
Room 207 A W - Session CPS+MS-MoA

Semiconductor Manufacturing Workforce Development

Moderators: Erica Douglas, Sandia National Laboratories, **Timothy Gessert**, Gessert Consulting

1:30pm **CPS+MS-MoA-1 Workforce Development in the Semiconductor Industry: A New National Approach***, **Michelle Williams***[1]*,* SEMI Foundation **INVITED**

To fulfill its promise to grow to $1 trillion as soon as 2030, the semiconductor industry will need an estimated 1 million new workers. Addressing this challenge will take a whole-of-industry, nationalized approach bolstered by significant federal and state investments. It will also require a fundamental rethinking of employer approaches to attracting, recruiting, and retaining a far broader workforce that represents the widest possible range of perspectives, backgrounds, and ideas so the industry can continue to innovate, problem solve, and thrive.

The SEMI Foundation is the workforce development arm of SEMI, the global industry association representing the microelectronics manufacturing and design supply chain with more than 3000 members worldwide. We know that accomplishing this work requires three strategies: we must illuminate and demystify the semiconductor industry for students and jobseekers; we must provide clear educational pathways into the industry; and we must provide access to hands-on training to prepare the workforce.

This keynote address will illuminate a new national approach on how to employ these strategies and weave them together to help galvanize a new generation of workers and create economic opportunity in communities proximate to semiconductor companies across the nation. Attendees will walk away with concrete and timely opportunities for their companies to engage in workforce development networks and activities to bolster their own success.

2:15pm **CPS+MS-MoA-4 Bridging the Talent Gap: Advancing Workforce Development for the Manufacturing and Semiconductor Industries***, **Sue Smith**,* Smart Automation Certification Alliance

The rapid advancement of technology and growing global demand for semiconductor components have placed unprecedented pressure on the U.S. manufacturing sector to expand and innovate. The landscape of geopolitics along with supply chain challenges have added to the mounting pressure. However, a widening skills gap combined with a shortage of an estimated 1.9 million manufacturing workers is most threatening to the industry's ability to meet this demand. This presentation addresses the urgent need for robust, scalable workforce development strategies tailored specifically to manufacturing and semiconductor manufacturing. Drawing on industry input, standards, and credential development, we will explore how partnerships among industry, government, and educational institutions can catalyze talent pipelines. The session will highlight successful case studies, outline key competencies for next-generation workers, and propose an ecosystem-based approach to building a resilient, diverse, and future-ready workforce. Attendees will gain actionable insights into curriculum innovations and collaborative models that can drive sustainable growth in one of the nation's most critical sectors.

The Smart Automation Certification Alliance (SACA) collaborates with partner companies in the manufacturing sector to develop credentials in Industry 4.0 and emerging technologies based on international standards supporting the attainment of certifications and demonstrated competencies. These credentials are being used by employers, secondary and post-secondary education, and training providers in developing the workforce for current and future skills needed in the workplace.

To effectively bridge the talent gap in the manufacturing workforce, particularly in emerging technologies like semiconductors, credentials will play a key role in an ecosystem-based approach. There are industry, government, and education partnerships having success in workforce development with SACA and other industry recognized credentials. More innovation and participation in collaborative models will drive sustainable solutions to addressing the skills gaps and meeting the demands for the growth in semiconductor production and advanced manufacturing. Development of standards by and for industry assures the appropriate skills and knowledge are identified and the attainment of aligned credentials develops the talent needed.

2:30pm **CPS+MS-MoA-5 Partnership of Research University and Technical College for Microelectronics and Nanomanufacturing Workforce Development***, **Seung-Joon Paik**, Yu "Michelle" Wu,* Georgia Institute of Technology*; Jameel Hasan,* Georgia Piedmont Technical College

A partnership has been established between the Georgia Institute of Technology, a research university with advanced nanomanufacturing facilities, and Georgia Piedmont Technical College, a technical college with regional professional education capabilities, aiming to address the nationwide demand for a workforce to build a talent pipeline for the semiconductor industry. Through this partnership, military veterans and their relatives are trained in a microelectronics and nanomanufacturing certificate program. The certificate program has achieved a completion rate of over 85% through 600+ hands-on lab hours using 20+ different pieces of equipment since 2022.

The U.S. semiconductor industry is projected to face a shortage of 53,200 engineers and technicians by 2030 due to the evolving demands of the industry according to The Semiconductor Industry Association. While many workforce development efforts are being invested to build education and training ecosystem, there are obstacles to overcome to accommodate workforce into the industry. Semiconductor fabrication or Nanomanufacturing facility has unique environments and requirements such as enclosed cleanrooms with stringent temperature, humidity and vibration, and head-to-toe covering cleanroom suit. Hands-on practices and proper training are crucial for enriching learning experiences and effectively applying job skills.

The Institute for Matter and Systems (IMS) at Georgia Institute of Technology is equipped with state-of-the-art nanofabrication machines and tools in a 28,500-square-foot space. Through the core facilities of cleanroom and material characterization, IMS offers hands-on training in lab safety, nanomanufacturing, and characterization to users. The capabilities include photolithography, thin film deposition, etch, and metrology, which are widely used techniques in high-tech nanomanufacturing industries and research facilities. Georgia Piedmont Technical College works as a hub of training opportunities for regional workforces in advanced manufacturing industries. The college engages military veterans in training programs for high-demand industries and implements education curricula and teaching methodologies in microelectronics and nanomanufacturing.

This presentation highlights a strategic partnership effort for workforce development in microelectronics and nanomanufacturing focused on veterans. Formation of partnership, modifications of curriculum, and hands-on experiences enriching students learning experience will be discussed. Key components involve successful approaches, lessons learned, and future access expansion.

2:45pm **CPS+MS-MoA-6 an Accelerated Bachelor's Degree in Semiconductor Materials and Devices***, Susan Farhat,* Department of Chemical Engineering, Kettering University*; Ronald Kumon, Daniel Ludwigsen, Uma Ramabadran, **Cornel Rablau**, Ronald Tackett, Demet Usanmaz, Lihua Wang,* Department of Natural Sciences, Kettering University

Kettering University, a STEM-focused private university in Michigan, is gearing up to launch an Accelerated Bachelor of Science degree in Semiconductor Materials and Devices that is designed to address one of the major hurdles in bringing semiconductor manufacturing back to the United States: a shortage of skilled workers. With the current strain on the global supply chain, and the CHIPS and Science Act injecting billions of dollars into bringing semiconductor manufacturing back to the US, the demand for highly-skilled professionals with semiconductor-industry-relevant training is skyrocketing. Funding for the development of this program has been obtained through a Strategic Investment Grant from the Michigan Economic Development Corporation (MEDC) intended to bolster Michigan's technological workforce. Kettering University has also become one of the participating schools under the MEDC-supported Michigander Scholars program to bolster workforce preparation in Michigan's high-tech sectors. The skill set required for a career in the semiconductor industry is inherently interdisciplinary, and this degree program reflects this, as it has elements from physics, chemistry, and engineering. In this talk, we will present the motivation behind this degree, the plan of study itself, and the reasoning behind why it was constructed in the manner in which it was.

[1] **Workforce Development Keynote Lecture**

3:00pm **CPS+MS-MoA-7 Building a Regional Education and Workforce Development Infrastructure for Semiconductor Manufacturing***, **Robert Geer,*** NY CREATES **INVITED**

The large-scale federal investments aimed at reasserting U.S. leadership in the global semiconductor industry has created an urgent need for a skilled IC design and manufacturing workforce. However, a significant talent gap threatens these goals. Addressing this need requires a comprehensive approach, currently underway, to build the education and workforce development infrastructure to support the semiconductor industry.

The Semiconductor Industry Association estimates that the industry will need to add more than 100,000 jobs in the U.S. to support planned or announced projects. Revitalizing the semiconductor talent pipeline requires a holistic approach. Nearly half the chip fab workforce will enter the industry with a high school diploma, 2-yr degree or non-credentialed training (e.g. military service). The remainder will be dominated by B.S./M.S./Ph.D. engineers, computer science, and research/development professionals. Addressing the challenges of preparing such a broad talent pool requires a combined national/regional strategy to address overall career awareness and engagement, modernization of training and education programming to address key skill and knowledge gaps, and targeted initiatives to reduce the 'time-to-productivity' for new hires.

A case study of this 'national/regional' strategy will be presented focusing on the new chip fabs under construction in the northeast U.S which will require tens of thousands of highly trained technicians, engineers, and data professionals over the next decade. The coordination of national initiatives (including the new National Semiconductor Technology Center in Albany, NY, regional DoD Microelectronics Commons Hubs in the northeast U.S. and Manufacturing U.S.A. institute investments) with regional (state-wide) efforts with in-depth analysis of competency profiles for semiconductor manufacturing will be reviewed in terms of maturing the region's workforce and educational ecosystem to support chip-fab expansion. Key components involve broadening the requisite competency base across the higher education network through industry-aligned curriculum modernization, expanded access to experiential learning in leading edge facilities, expanded adoption of 'learn and earn' opportunities and coordination with national awareness campaigns. Central to this strategy is the role played by industry organizations and regional development nonprofits as a 'connective tissue' to support the overall talent pipeline.

3:30pm **CPS+MS-MoA-9 Workforce Development Opportunities in a University Nanofabrication Core Facility***, **Megan Dernberger**, Benjamin Schmidt, Christina McGahan, Sarah Ross, Sharon Weiss,* Vanderbilt University

In Vanderbilt Institute of Nanoscale Science and Engineering (VINSE) at Vanderbilt University, several programs are successfully implemented to engage students, postdocs, and external users of VINSE in workforce development. Programs include workshops, an Industrial Affiliates Program (IAP), and part-time student employment. These programs are mutually beneficial to staff and users, reducing the time burden for full-time staff while also promoting users' technical, teaching, and leadership skills. This talk highlights lessons learned with the development of these programs.

The VINSE IAP fosters collaborative relations with industry leaders. This program allows students and faculty direct access to industry contacts for recruitment, job opportunities, and networking events. The industry members can sponsor workshops with technical trainings, interactive Q&A sessions, and content tailored to the userbase. Utilizing connections with VINSE alumni and a modest entry fee to create a low barrier to entry resulted in over 15 IAP members in the first year.

Additionally, VINSE offers staff-led short courses to the internal and external community. The one- or two-day events provide a hands-on introduction into topics and technical skills for users. Topics include microfluidic device fabrication, semiconductor device fabrication, electron microscopy, and atomic force microscopy.

Undergraduate and graduate students can be directly involved in VINSE for months to years through the VINSE Undergraduate Tech Crew and SuperUser programs respectively.Tech Crew undergraduates, ~14, assist staff with cleanroom upkeep and process development. They specialize in various tools and processes, gaining hands-on experience and exposure to a wide range of nanoscience applications. Students can join Tech Crew during an intensive 10-week summer program or the academic year. A three-level tiering system acknowledges skill and leadership development with promotions in title, pay, and responsibilities.Graduate student SuperUsers, ~5, are selected based on technical and interpersonal skills and assist with highly-used cleanroom equipment. They provide initial tool training to users and initial troubleshooting of tool issues on a subset of tools, building teaching experience and deeper tool knowledge. As an incentive, SuperUsers have increased access to VINSE staff, extra training on selected tools, and a professional development stipend.

These workforce development programs are highly successful for fostering interdisciplinary relations, increasing technical skills, and enhancing the nanoscience research community at Vanderbilt.

4:00pm **CPS+MS-MoA-11 Challenges of Infusing Vacuum Technology into Two-Year Technology Programs***, **Elena Brewer,*** Erie Community College

With the recent revival of semiconductor manufacturing in the United States, the industry is challenged with the lack of a qualified technical workforce to meet the rapidly growing demand for technicians.Vacuum technology has a special place of being an enabling technology for the semiconductor industry and other industry segments.Thus, the availability of technicians prepared to work with and troubleshoot vacuum-based systems is essential for the semiconductor industry.This presentation will address the challenges encountered by SUNY Erie Community College and Normandale Community College, and present corresponding solutions to overcome these challenges.The main three challenges in teaching vacuum technology at the community college level are: lack of institutional expertise, lack of available training equipment, and lack of technician-level educational resources in vacuum technology.SUNY Erie has been tackling these challenges since 2014 when ECC's Nanotechnology AAS program was first introduced. Since then, vacuum technology has been infused into the Electrical Engineering Technology AAS program, and a standalone Vacuum Technology micro-credential was developed. Normandale Community College has been working on providing educational solutions in Vacuum Technologies even longer and offers vacuum technology training at various levels using different modes of course delivery, including interactive remote-access vacuum instruction. This presentation will highlight the educational resources developed over multiple NSF ATE grant projects that are available for community college and technical college faculty, such as: an eBook in Vacuum Technology; laboratory manual and instructor's guide to support experiential learning in Vacuum Technology; rough and high vacuum technology training equipment; and current and future professional development opportunities for community college and technical program faculty.

4:15pm **CPS+MS-MoA-12 Review of AVS Educational Outreach Activities in the Context of the Chips in Science Act and its Related Workforce-Development Needs***, **Tim Gessert,*** Gessert Consulting LLC

The AVS has provided various types of education opportunities to its members and others since the mid 1960's. One important component of these activities has been public and private *short courses*on topics consistent with the needs of various high-technology sectors. Indeed, for many technologists, engineers, and scientists now working in these high-tech industries, their initial exposure to areas such as basic vacuum technology, vacuum-process development, and characterization, often began with an AVS Short Course. In the mid 1980's, AVS education outreach expanded to include training high-school teachers through the *AVS Science Educators Workshop* (SEW). Through this activity, many hundreds of high-school teachers throughout the U.S. have received not only basic vacuum training, but also a working vacuum system designed for the needs of a high-school classroom. In addition to the SEW helping these teachers convey the extensive uses of vacuum processes in many industries, another goal of the SEW has always been to help "spark" student interest in considering post-secondary education (i.e., college), and possibly even toward an STEM career involving vacuum technology. Recently, and encouraged by the realities of COVID, many AVS education outreach activities now also include the option for virtual training, including virtual short courses, webinars, and You-Tube videos that can often align better with changing workplace and workforce needs. Additionally, in partnership with the American Institute of Physics (AIP), the AVS is now actively exploring how to better provide this type of education outreach to communities that have been historically underrepresented in the high-technology sectors.

In this presentation, the past ~60 years of AVS experience with educational outreach will be briefly reviewed, emphasizing how these ongoing activities and experiences might be leveraged to benefit the workforce development needs of the Chips in Science Act. It will also be discussed how, while the workforce of the future US Semiconductor Workforce will certainly require many skilled individuals with advanced academic degrees, this future workforce will continue to require many individuals with hands-on technology skills in areas such as process development/optimization and

equipment operation/maintenance. Because of the long-term AVS experience with training involving all these different workforce sectors, it is believed that much of the established AVS education outreach activities can significantly benefit the activities related to the Chips in Science Act.

Electronic Materials and Photonics
Room 207 A W - Session EM1+AP+CPS+MS+PS+QS+SM+TF-TuM

Emerging Frontiers in Quantum Materials and Devices
Moderator: Mollie Schwartz, MIT Lincoln Laboratory

8:30am **EM1+AP+CPS+MS+PS+QS+SM+TF-TuM-3 Rapid, Atomic-Scale Smoothing of GaSb(111)A Surfaces During Molecular Beam Epitaxy**, ***James Rushing***, *Paul Simmonds,* Tufts University

InAs/Ga(In)Sb quantum wells (QWs) with a broken gap band alignment can behave as a quantum spin hall insulator (QSHI) with an insulating bulk and topologically protected helical edge states [1-2]. QSHIs could be a key component in spintronic and topological quantum computing applications [2-3]. Producing a topological phase transition in InAs/Ga(In)Sb QWs requires precise control of QW thickness, composition and quality, particularly at the heterointerfaces. Additionally, our calculations suggest QWs grown on (111) surfaces could provide benefits over (001) due to the higher symmetry and out-of-plane polarization effects of this surface.

While exploring the MBE growth of InAs/Ga(In)Sb QW heterostructures on GaSb(111)A, we discovered an exciting and confounding phenomenon that seems to be unique to crystal growth on III-Sb(111)A surfaces. Ga(In)Sb(111)A frequently exhibits an extremely rough morphology characterized by pyramidal peaks covering the entire surface. We show that rough III-Sb surfaces (pyramidal features >70nm in height; rms roughness >10nm), can be smoothed to atomically flat surfaces (<3nm height features; <0.5nm rms roughness) in a matter of seconds by exposing them to an arsenic over-pressure. We first observed this phenomenon when rough GaInSb(111)A surfaces became atomically flat after capping with just 8nm of InAs. After reducing the thickness of this InAs layer to a single monolayer and still observing he same surface smoothing effect, we found that we could achieve almost identical results by simply exposing the rough GaSb(111)A to an arsenic flux. These results suggest that arsenic is the primary mover in these profound morphological changes. Our recent results show that the smoothing can be accomplished with As_4 or As_2, and with a wide range of arsenic beam equivalent pressures, from $5x10^{-7}$ to $1x10^{-5}$ Torr.

We will describe our efforts to gain control and understanding of this phenomenon through the modulation of arsenic exposure time, flux, and terminating III-Sb material. This powerful new MBE technique will allow us to reliably achieve smooth heterointerfaces in (111)-oriented InAs/Ga(In)Sb QWs for novel, high-quality QSHIs. More broadly, we believe that this approach will enable the growth of a wide array of III-Sb-based nanostructures on (111)A surfaces for other electronic and photonic applications.

1. Krishtopenko and Teppe. *Science Advances* **4**, eaap7529 (2018)
2. Avogadri et al. *Physical Review Research* **4**, L042042 (2022)
3. Du et al. *Physical Review Letters* **119**, 056803 (2017)

8:45am **EM1+AP+CPS+MS+PS+QS+SM+TF-TuM-4 Benchmarking Different NbTiN Sputtering Methods for 300 mm CMOS-compatible Superconducting Digital Circuits**, *Adham Elshaer*[1], ***Jean-Philippe Soulié***, *Daniel Perez Lozano, Gilles Delie, Ankit Pokhrel, Benjamin Huet,* IMEC Belgium*; Margriet J. Van Bael,* KU Leuven and Imec, Belgium*; Daan Buseyne,* KU Leuven, Belgium*; Blake Hodges, Seifallah Ibrahim, Sabine O'Neal,* Imec USA*; Zsolt Tökei,* Imec Belgium*; Anna Herr, Quentin Herr,* Imec USA

The NbTiN films presented here are CMOS-compatible and were developed for metallization purposes in superconducting digital circuits [1-5]. Those circuits use NbTiN for Josephson junctions and capacitors electrodes, as well as for wiring. Superconducting digital circuits initially relied on Nb in the early days. NbTiN is a better candidate/replacement due to its higher thermal budget and better chemical stability [1-5]. In this study, the properties of superconducting NbTiN thin films deposited using two different sputtering methods have been compared. One method used multiple targets (MT) co-sputtering (Nb and Ti targets), while the other used a NbTi single target (ST). Benchmarking metrics used for comparison include: superconducting, electrical, as well as morphological properties. All films show a high Tc, ranging from 13.3 K to 15.1 K. Compared to MT, ST NbTiN films showed consistently lower resistivity and better sheet resistance (Rs) wafer-level uniformity (49 points wafer-map). For instance, 50 nm MT film had a Rs relative standard deviation (Stddev%) of 15.5%, while for the ST NbTiN films, Rs Stddev% showed a 2-fold improvement at 7.8%. Upon annealing of the ST NbTiN films at 650℃, the Rs uniformity further improved, reflected by a lower Stddev% at 4.5%. AFM data show similar results for MT and ST films, ~1.07 nm and 1.09 in the center and 0.73 nm and 0.71 nm at the edge of the wafers, respectively. Furthermore, XRD theta-2theta scans have been performed showing the 200 and 111 peaks for NbTiN orientations. Results show that the MT and ST films have different/signature 200/111 peak intensity ratios for the as deposited films. ST NbTiN films have a lower 200/111 peak ratio. However, after annealing at 650℃, the ST films 200/111 peak ratio increases, and surpasses that of the MT NbTiN films. This change suggests a change in the ST film disorder and grain size after annealing. The impact of the ST NbTiN film thickness on properties has also been studied. The Tc shows an increase as a function of thickness, from 9.6 K for 7 nm, to 14.3 K for 50 nm, up to 14.9 K for 200 nm films. Certainly, the ability to tune the superconducting properties of NbTiN, makes them appealing from a stack engineering perspective. Both MT and ST NbTiN properties can be tailored using deposition conditions such as: power, partial pressure and post deposition annealing [3]. However, MT NbTiN films 300 mm wafer-level Rs non-uniformity represents a limiting factor for scaling superconducting devices. Annealed NbTiN ST films on the other hand, show a 3.4-fold Rs wafer uniformity improvement while maintaining properties tunability.

9:00am **EM1+AP+CPS+MS+PS+QS+SM+TF-TuM-5 Controlling the Properties of Epitaxially Grown Topological Semimetals**, ***Kirstin Alberi***, National Renewable Energy Laboratory **INVITED**

Three dimensional topological semimetals (TSMs) exhibit a wide range of interesting properties, including high carrier mobility, large magnetoresistance, anomalous transport behavior, broadband optical absorption and non-linear optical responses. Epitaxial thin film synthesis offers a practical platform for manipulating composition, defects and disorder in these materials, offering a window into approaches for manipulating their properties. In this talk, I will discuss insights into the relationships between structure and composition and the resulting properties revealed through careful control of growth conditions. Focused examples include the impact of point defects and impurities on electron transport in the Dirac TSM Cd_3As_2 and the formation and behavior of domain boundaries in the Weyl TSM TaAs.

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9:30am **EM1+AP+CPS+MS+PS+QS+SM+TF-TuM-7 Photon Down-Conversion of Yb-Doped CsPb(Cl1-xBrx)3 to Low-bandgap Metal Halide Perovskites**, ***Yutong Ren***[2], Princeton University*; Igal Levine,* The Hebrew University of Jerusalem, Israel*; Dan Oron, David Cahen,* Weizmann Institute of Science, Israel*; Antoine Kahn,* Princeton University

Quantum cutting represents a transformative strategy to mitigate thermalization losses that typically occur when high-energy photons are absorbed by semiconductors.[1,2] Recent advances have extended this concept from rare-earth doped crystals to semiconductor–rare-earth hybrid systems, particularly those utilizing halide perovskite absorbers, thereby exploiting their exceptional optoelectronic properties.

In this study, we focus on Ytterbium (Yb) -doped $CsPb(Cl_{1-x}Br_x)_3$, a metal halide perovskite that absorbs visible light and exhibits intense near-infrared (NIR) photoluminescence—a clear signature of efficient quantum cutting. Upon excitation with visible light, the doped perovskite converts the absorbed energy into two NIR photons, with the emission energy closely matching the optimized bandgap of a Sn–Pb based perovskite absorber. This spectral alignment is critical for enabling effective energy transfer between the quantum cutting layer and the absorber.

[1] **JVST Highlighted Talk**

[2] **JVST Highlighted Talk**

Our investigation focuses on elucidating the structural and electronic properties of the interfaces between Yb-doped $CsPb(Cl_{1-x}Br_x)_3$ and Sn–Pb based perovskite films. By employing a suite of advanced spectroscopic techniques—including ultraviolet photoelectron spectroscopy, inverse photoemission spectroscopy, time-resolved photoluminescence (tr-PL), and time-resolved surface photovoltage (tr-SPV)—we systematically examine how the quantum cutting layer, the absorber layer, and their interfacial region collectively influence energy transfer efficiency. In particular, the complementary tr-PL and tr-SPV analyses unambiguously determine the dominant interfacial charge transfer and recombination processes, and thus gain control over the interfacial charge transfer. By integrating Yb-doped $CsPb(Cl_{1-x}Br_x)_3$ with customized Sn–Pb perovskite absorbers, our approach shows promise for pushing the boundaries of conventional efficiency limits while also offering a cost-effective strategy for enhanced energy conversion.

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9:45am **EM1+AP+CPS+MS+PS+QS+SM+TF-TuM-8 Molecular Beam Epitaxy Growth of $InAs_{1-x}Bi_x$ on GaSb for Topological Insulating States***, **Merve Baksi**, James Rushing, Xikae Xie, Avery Hanna, Larry Qui, Ekow Williams, Paul J. Simmonds,* Tufts University

Incorporation of bismuth (Bi) into III-V semiconductors has attracted significant interest not only for its ability to extend infrared optoelectronic applications across a wide spectral range but also for its potential to induce topologically protected surface states, which could form the foundation for certain quantum computing technologies [1].

Motivated by the small inverted band gap that can be induced in InAs/GaSb quantum wells (QWs) [2], we propose engineering the band structure and inducing the edge states through Bi incorporation into InAs layers. This enhancement is expected to improve robustness against thermal fluctuations, making the material viable for room temperature applications as opposed to the topological HgTe/CdTe QW system with a temperature dependent band gap [3].

Theoretical studies predict that $InAs_{1-x}Bi_x$ quantum wells exhibit a topological insulating state when the Bi composition reaches $x \approx 0.15$, with an estimated inverted gap of approximately 30 meV [1]. Given these predictions, InAsBi emerges as a promising candidate for realizing two-dimensional topological insulators (2D TIs). However, achieving such high Bi incorporation remains challenging due to the significant miscibility gap and the limited solubility of Bi in III-V materials [4].

In this work, we investigate the molecular beam epitaxy (MBE) growth of InAsBi on GaSb substrates, focusing on optimizing Bi incorporation and structural quality. By leveraging MBE growth techniques, we aim to systematically control Bi incorporation and assess its impact on electronic and structural properties of InAsBi in reduced dimensions. Our findings will contribute to the advancement of III-V-based topological materials and their potential integration into future quantum devices.

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Electronic Materials and Photonics
Room 207 A W - Session EM1+CPS+MS+PS+SM+TF-TuA

Advances in Materials and Processes for Devices and Interconnects (FEOL and BEOL)

Moderators: Moon Kim, University of Texas at Dallas, **Philip Lee**, University of Kentucky

2:15pm **EM1+CPS+MS+PS+SM+TF-TuA-1 Carborane-Based Blocking Layers and Plasma Removal Strategies for Area Selective Deposition in Semiconductor Patterning**, ***Raja Sekhar Bale***, University of Missouri-Kansas City; *Rupak Thapa,* University of Missouri-Kansas City; *Vamseedhara Vemuri, Nicholas Strandwitz,* Lehigh University; *Anthony Caruso, Michelle Paquette,* University of Missouri-Kansas City

Advancing semiconductor scaling to the 2 nm and angstrom-level nodes requires patterning methods that move beyond the resolution, alignment, and cost limits of conventional top-down approaches. Area-selective deposition (ASD) provides a complementary bottom-up strategy, enabling growth only where desired to reduce process steps, minimize defects, and/or improve integration in back-end-of-line (BEOL) fabrication. This work investigates the use of carborane self-assembled monolayers (SAMs) as blocking layers for ASD. Carborane SAMs are thermally stable, mechanically robust, and chemically tunable, making them strong candidates for selective surface modification in semiconductor patterning. Their role is to define surfaces where deposition should be inhibited, while remaining compatible with BEOL conditions. To explore their processing compatibility, the blocking ability of carborane SAMs toward ALD dielectric oxides was studied alongside plasma-based removal. Using CF_4/O_2 and C_4F_8/O_2/Ar chemistries, we carried out blanket plasma etching of carborane SAMs. This presentation will highlight results on carborane SAM formation, blocking behavior, and plasma response, demonstrating their potential as scalable materials for atomic-scale patterning in next-generation semiconductor manufacturing and their compatibility with advanced BEOL integration.

2:30pm **EM1+CPS+MS+PS+SM+TF-TuA-2 Ferroelectricity in Atomic Layer Deposited Wurtzite Zinc Magnesium Oxide Zn1–xMgxO**, ***Benjamin Aronson***, University of Virginia; *Kyle Kelley,* Oak Ridge National Laboratory; *Ece Gunay,* Carnegie Mellon University; *Ian Mercer,* Penn State University; *Bogdan Dryzhakov,* Oak Ridge National Laboratory; *Susan Trolier-McKinstry, Jon-Paul Maria,* Penn State University; *Elizabeth Dickey,* Carnegie Mellon University; *Jon Ihlefeld,* University of Virginia

Ferroelectric wurtzites have garnered interest in the scientific community since first reported in 2019. $Zn_{1-x}Mg_xO$ has shown promise due its low coercive field (2–3 MV/cm) relative to other wurtzites, integrability on flexible polymer substrates, and complementary metal–oxide–semiconductor (CMOS) and back–end–of–line (BEOL)compatible deposition temperatures as low as room temperature. However, the majority of ferroelectric wurtzite thin films – including $Zn_{1-x}Mg_xO$ – have been fabricated using physical vapor deposition (PVD) techniques, which features largely directional growth. Due to the use of high aspect ratio structures in non–volatile memory devices, the ability to conformally deposit ferroelectric wurtzites will contribute to BEOL integration. Atomic layer deposition (ALD) presents an opportunity to overcome this outstanding challenge due to its sequential, self–limiting growth. In this work, $Zn_{1-x}Mg_xO$ thin films with compositions between x = 0 and x = 0.58 were grown on platinized silicon substrates using plasma–enhanced atomic layer deposition. Films were characterized using X–ray diffraction (XRD), transmission electron microscopy (TEM), and piezoresponse force microscopy (PFM). All films deposited featured a singular out–of–plane c–axis textured wurtzite structure. The c/a ratio decrease with increasing Mg content indicates the increasing structural distortion. Film structure and structural distortions were further reinforced and visualized via TEM. PFM amplitude and phase hysteresis loops demonstrated polarization reversal in the x = 0.46 and x = 0.58 films. Ultimately, this finding presents opportunities to further mature the $Zn_{1-x}Mg_xO$ processing space in which ferroelectric switching is possible, as well as explore ALD of other ferroelectric wurtzites.

2:45pm **EM1+CPS+MS+PS+SM+TF-TuA-3 Harnessing Nitrogen-Rich Interfaces in AlN Ferroelectrics**, ***Ian Mercer***[1], *Erdem Ozdemir, Chloe Skidmore, Benjamin Debastiani, Kazuki Okamoto,* Penn State University; *Sebastian Calderon, Elizabeth Dickey,* Carnegie Mellon University; *Susan Trolier-McKinstry, Jon-Paul Maria,* Penn State University

The importance of interface preparation in the nitride semiconductor and thin film community has long been recognized as critical in controlling nucleation and properties. These AlN ferroelectrics are an enticing pathway toward integrated energy-efficient robust non-volatile memory, displaying CMOS chemical compatibility, large polarizations, and BEOL processing. Although this has not been fully realized in the relatively recent nitride wurtzite ferroelectric community, current convention stems from strictly polar systems like GaN and AlN. However, there is a clear opportunity in engineering electrode interfaces in these systems to aid in film nucleation, reduced leakage, and extended fatigue lifetimes. In this work, we discuss the influence of surface nitriding on a variety of relevant substrates prior to film deposition to enhance film texture and electrical properties. Adding the surface nitriding leads to a discussion on whether nitrogen-rich interfaces can compensate for nitrogen vacancies that migrate to electrode interfaces during cycling. By depositing top and bottom metal nitride electrodes, we investigate the benefits in the electrical properties versus metallic electrodes. Reactive RF magnetron sputtering is employed to co-sputter AlN ferroelectrics. X-ray diffraction (XRD) is used to display *c*-axis texture, while hysteresis (PE), leakage (PUND), and fatigue measurements are used to characterize the electrical properties. Etching/SEM is also used to display partial switching, exploiting the n-polar fast etch in KOH solutions, which helps visualize the effects of nitrogen-rich interfaces. Furthermore, this study reinforces the functionality of interface engineering in AlN ferroelectrics at both the top and bottom electrode interfaces. The importance of this work is that all films in this class may benefit from nitrogen-rich interfaces.

3:00pm **EM1+CPS+MS+PS+SM+TF-TuA-4 Selective Etching of GaN Over AlGaN and Monitoring via Optical Emission Spectroscopy**, ***Michael Thomas***, *Patrick Wellenius, Spyridon Pavlidis,* North Carolina State University

Achieving etch selectivity between GaN and AlGaN is critical for the repeatable fabrication of enhancement-mode AlGaN/GaN High Electron Mobility Transistors (HEMTs). The selectivity can be tuned by varying the O_2 content in a Cl_2-based etch. In this work, we explore the etch process parameter space that affects selectivity and explore how *in-situ*optical emission spectroscopy (OES) can be used as an indicator of chamber and plasma conditions over time.

Two epitaxial structures on sapphire were used. The first is a thin film of GaN (control). The second is a device-relevant AlGaN/GaN heterojunction with a GaN cap layer**.** Following photolithography,samples of each type were etched simultaneously in an Oxford Instruments Plasmapro 100 Cobra inductively coupled plasma (ICP) to eliminate run-to-run variation from the selectivity determination. The total etch time was varied by gas composition to keep the HEMT sample etch depth within the AlGaN front barrier. Etch step heights were measured via atomic force microscopy (AFM) in an Oxford Instruments Asylum Research MFP-3D Origin AFM. Using an OceanOptics USB4000 Spectrometer, OES signals were collected with 1 s integration every 60 s during chamber cleaning and conditioning, and every 30 s during the final etches for each composition.

During initial experiments, the chamber pressure, ICP power, and table RF power were all kept constant at 15 mTorr, 500 W, and 25 W, respectively. The total gas flow was kept constant at 50 sccm, and Cl_2 was further kept constant at 35 sccm. The remaining 15 sccm were split between O_2 and Ar, with three tests being done at 0/15, 2/13, and 4/11 sccm of O_2/Ar respectively. An initial peak selectivity of 3.45:1 was measured with 2 sccm O_2. The OES signalconfirms O_2 emission brightness changes as expected with flow rate. To further improve the selectivity, we will report on the etch characteristics across a wider parameter space, including varying the Cl_2 content of the plasma, the total gas flow rate, the chamber pressure, ICP power and substrate size. Moreover, we explore how the OES's utility can be leveraged to assess the effectiveness of pre-etch chamber conditioning to improve both selectivity and repeatability. The results of this study are expected to boost the yield and performance of AlGaN/GaN HEMTs.

This technology was primarily supported by the Microelectronics Commons Program, a DoD initiative, under award number N00164-23-9-G059.

[1] **JVST Highlighted Talk**

Electronic Materials and Photonics

Room 207 A W - Session EM2+AIML+AP+CPS+MS+SM-TuA

Advances in AI and Machine Learning within the Semiconducting Industry

Moderator: Erica Douglas, Sandia National Laboratories

4:00pm **EM2+AIML+AP+CPS+MS+SM-TuA-8 Improved Design-of-Experiments and Process Modeling with Generative AI***, **Somilkumar Rathi,** Muthiah Annamalai,* Panmo LLC

Small volume semiconductor, photonic and materials manufacturing largely uses One-Factor at-a time (OFAT) to discover process window instead Design of Experiments (DOE). We demonstrate, *Panmo Confab,* a Generative AI based DOE and process-flow-design platform to accelerate process window discovery. Large volume semiconductor, photonic and materials automation tools have relied on statistical process control (SPC), design of experiments (DOE) and yield modeling techniques which are fairly manual and depend on specialized tools and deep knowledge [1,2]when such tools are not used we get a sub-optimal outcomes for process development teams through using one-factor at a time (OFAT). In this article we report, and demonstrate, *Panmo Confab* a Generative AI based process flow tracking and design of experiments platform to accelerate flow designs and generating DOEs. Previously our tool was used without Generative AI, features to show improvement in process discovery for plasmonic nanocavity fabrication [4]. The unique innovation of our tool is to use the emerging technology of large language models (LLM), like BERT or ChatGPT [5,6] and science of causality [3] to enable generation of process flows with a description. Our tool is presented in both on-premises and Software-as-a-Service (SaaS) formats.

References:

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4:15pm **EM2+AIML+AP+CPS+MS+SM-TuA-9 Foundation Models in Semiconductor R&D: A Study on Segment Anything***, **Fei Zhou,*** Sandisk Corporation

Quantitative analysis of scanning and tunneling electron images is crucial in semiconductor manufacturing, particularly for defect detection, process margin checking, and morphology quantification. Traditional AI/ML approaches, such as using recurrent neural networks, require large labeled datasets and extensive transfer learning to generalize across different imaging conditions. Developing a usable AI tool for proof-of-concept demonstrations demands significant engineering effort and GPU resources, making these methods costly and time-consuming. These challenges are especially pronounced in semiconductor R&D, where fast turnaround, high accuracy, and efficient use of engineering resources are essential.

The Segment Anything Model (SAM) introduces a novel training free segmentation approach, eliminating the need for task-specific retraining while providing robust and efficient segmentation across diverse semiconductor imaging requirements. This paper explores SAM's application in semiconductor image analysis, demonstrating its ability to segment complex nanoscale features without prior dataset exposure. We assess SAM's performance in automated defect detection, where challenges such as varying defect morphology, background noise, and process-induced variations exist. With appropriate prompting and post-processing techniques, SAM adapts to different imaging conditions, offering a rapid, low-cost, and high-accuracy solution.

Additionally, we examine SAM's limitations, particularly in scenarios where the region of interest is small and contains limited useful pixel data. By employing image enhancement techniques, we demonstrate how SAM can effectively segment defects even in low-information conditions. Furthermore, we explore how integrating grounding techniques with SAM can expedite segmentation post-processing, further improving efficiency in real-world applications.

Our case studies show that SAM significantly reduces resource overhead and enables semiconductor image analysis automation, achieving saving of >100 engineering hours and >20 GPU hours per project. Its foundation model architecture allows it to generalize across different defect types, backgrounds, and imaging techniques without additional data labeling or fine-tuning. These findings suggest that integrating SAM into semiconductor workflows enhances efficiency, lowers costs, and accelerates R&D decision-making by providing a scalable and cost-effective solution for high-precision image segmentation. This study highlights the transformative potential of foundation models in semiconductor engineering, paving the way for broader adoption of AI-driven automation across the industry.

4:30pm **EM2+AIML+AP+CPS+MS+SM-TuA-10 MOFCreatioNN: A Novel Modular Machine Learning Approach for Designing 'Undesignable' Metal-Organic Frameworks.** , ***Satya Kokonda,*** Charter School of Wilmington

Many critical material discovery processes remain too complex for traditional computational modeling, necessitating costly and time-intensive experimentation. Here, we present a generalizable, application-driven methodology for material design, demonstrated through a case study in photocatalysis. Using a reinforcement learning ensemble, we generated 120,000 novel metal-organic frameworks (MOFs) optimized for CO_2 heat of adsorption and CO_2/H_2O selectivity. A multi-objective fitness function—incorporating stability, catalytic potential, cost, sustainability, and adsorption properties—enabled computational modeling of photocatalytic performance aligned with industrial criteria. To enhance efficiency and prevent feature overfitting, a predictor funnel system iteratively filtered low-scoring candidates, narrowing the search space to 17,315 MOFs and improving computational efficiency by 313%. Our system, MOFCreatioNN, designed two high-performing, de novo MOFs: a Cr-based MOF with a photocatalyst score 239% higher than the control, and a Mn-based MOF that outperformed all baselines across every evaluated metric, demonstrating robustness against imperfect fitness functions. The proposed MOFs meet key synthesis and operational thresholds—including X-ray diffraction consistency with known structures, predicted synthesizability, temperature stability >300°F, and viable water stability—making them practical for real-world applications. Furthermore, we identify actionable design heuristics, such as the significant impact of the $N_2$62 metal cluster on photocatalytic performance. By integrating industrial considerations such as cost, stability, and environmental viability into the modeling process, this work showcases a scalable framework for the AI-driven design of industrially relevant materials in domains previously considered computationally intractable.

Electronic Materials and Photonics
Room 207 A W - Session EM1+AP+CA+CPS+MS+TF-WeM

Advances in Wide Bandgap Materials and Devices
Moderator: Erin Cleveland, Laboratory of Physical Sciences

8:00am **EM1+AP+CA+CPS+MS+TF-WeM-1 Progress in Wide and Ultra-Wide Bandgap Semiconductors – Energy Implications**, ***John Muth,*** North Carolina State University **INVITED**

The progress in developing wide bandgap semiconductors from idea to commercial products over the past 30 years is one of the great successes of interdisciplinary research between materials, science, physics and electrical engineering. Presently, we are experiencing another step change in the performance of semiconductor devices as ultra-wide bandgap materials (Diamond, Aluminum Nitride, Gallium Oxide) overcome fundamental issues like wafer size, the ability to control conductivity with doping in controlled ways and techniques like wafer bonding become more widely used and high voltage device demonstrations are being made. Similarly, SiC and Gallium Nitride wide bandgap devices are leveraging more mature fabrication technologies including deep ion implantation, sophisticated etching techniques, and high k dielectrics to enable non-planar device geometries, that lower the on resistances and provide increased breakdown voltages. The use of emerging alloys like AlScN offer higher performance higher frequency transistors as well as an addition route to integrate ferroelectric materials with CMOS. Innovations in photonic devices should not be left out with microLEDs for displays and chip to chip communications and increased ability to make low loss visible photonic integrated circuits as well as narrow linewidth lasers for quantum. The goal of this presentation will be to put these advances into context comparing the advances in the different materials and their potential for energy savings for a variety of systems including Artificial Intelligence, Data Centers, and computing and systems where size, weight, power efficiency and reliability matter including ships, planes and satellites.

8:30am **EM1+AP+CA+CPS+MS+TF-WeM-3 Limitations and Effects of Heavy Metal Doping in GaN**, *J. Pierce Fix,* Montana State University*; Kevin Vallejo,* Idaho National Laboratory*; Nicholas Borys,* Montana State University*;* ***Brelon May,*** Idaho National Laboratory

The doping of third-party elements is the backbone of the microelectronics industry, as it allows delicate control of electron/hole concentration, but it can also be used to imbue a host matrix with unique magnetic or optical properties. Wurtzite gallium nitride is a widely studied large bandgap semiconductor. There are reports of doping GaN with numerous elements, with some being extensively employed in commercial applications. However, there are still a few elements which remain completely unexplored. This work investigates the doping limits and effects of select transition metals, lanthanoids, and actinoids in GaN. The structural, electronic, and optical properties of these first-of-a-kind combinations are presented. Embedding single crystal wide bandgap materials with additional functionality will provide building blocks for new multifunctional hybrid systems for novel sensors, quantum science, or meta-multiferroics. Leveraging the non-centrosymmetric piezoelectric host matrix and atomic-level control of dopant species could allow for active tuning of proximity and correlated phenomena, potentially opening the door for applications of actinide elements beyond nuclear fuels.

8:45am **EM1+AP+CA+CPS+MS+TF-WeM-4 Using Raman Spectroscopy to Characterize Stress and Strain in SiC**, ***Michelle Sestak,*** HORIBA

Raman spectroscopy is a useful, non-destructive tool for measuring stress and strain in materials like silicon carbide (SiC). In this study, we use Raman spectroscopy to analyze stress and strain in three types of SiC samples: as-cut, diamond-lapped, and after chemical mechanical polishing (CMP). By examining shifts in the Raman peak positions, we identify differences in residual stress caused by each processing step. The as-cut samples show high stress due to mechanical damage, while diamond-lapped samples show partial stress relief. The CMP-treated samples exhibit the lowest stress levels, indicating effective surface relaxation. These results demonstrate how Raman spectroscopy can be used to monitor and compare the effects of different surface preparation techniques on stress in SiC materials.

9:00am **EM1+AP+CA+CPS+MS+TF-WeM-5 Nanoscale GaN Vacuum Electron Devices**, ***George Wang,*** *Keshab Sapkota, Huu Nguyen, Gyorgy Vizkelethy,* Sandia National Laboratories

On-chip vacuum electron devices that operate by cold field emission have the potential to combine advantages of traditional vacuum electron devices (e.g. vacuum tubes), such as robustness in harsh environments and high frequency operation, together with those of modern solid-state devices, such as size and energy efficiency. By shrinking the vacuum or “air” channel to nanoscale dimensions well below the electron mean free path in air, such devices can operate at ambient pressures while maintaining the physical advantages of ballistic vacuum transport. Here, we present lateral gallium nitride (GaN) semiconductor nanogap field emission diodes and transistors that exhibit ultra-low turn-on voltage, high field-emission current, and that operate in air. The fabrication of these nanoscale devices is enabled by a two-step top-down etching approach allowing for the necessary sidewall verticality and surface smoothness. We present experimental and modeling results on the field emission characteristics of these devices at various nanogap sizes and operating pressures. Initial results showing the potential of these devices for radiation-hardened, photodetection and high-temperature applications will be presented. These results provide critical new insights into the behavior of this new class of devices and point to future challenges and opportunities. *Sandia National Laboratories is managed and operated by NTESS under DOE NNSA contract DE-NA0003525*

9:15am **EM1+AP+CA+CPS+MS+TF-WeM-6 Combining CVD of Graphene and SiC for Efficient Layer Transfer**, ***Daniel Pennachio,*** *Jenifer Hajzus, Rachael Myers-Ward,* US Naval Research Laboratory

Remote epitaxy (RE) is a thin film growth technique that incorporates a release layer into the material stack, allowing for transfer of the deposited material with minimal defects [1]. Transferred 2D two-dimensional (2D) material, such as graphene, is commonly used for a release layer, but the transfer step can degrade the film and increase process complexity. To avoid this, we examine *in situ* graphitic carbon growth on SiC substrates before subsequent SiC epitaxy in the same chemical vapor deposition (CVD) RE process. RE SiC and subsequent SiC epilayer transfer is desired since isolated SiC membranes are excellent for quantum photonics and SiC substrate reuse can provide significant cost savings. Despite these benefits, the high-temperature hydrogen-containing CVD environment can damage graphene, making RE difficult under standard SiC growth conditions [2].

This study established growth windows for *in situ* graphene via propane-based hot wall CVD. This propane-based graphene growth enables an efficient transition to subsequent SiC deposition using established SiC growth conditions since it shares a similar hydrogen ambient to standard SiC CVD. Growing at 1620 °C in 20 slm H_2 with 20 sccm propane flow produced predominantly monolayer (ML) graphene films on on-axis 6H-SiC(0001) substrates with minimal defects found in Raman spectral maps. Films grown on 4° off-axis 4H-SiC(0001) substrates were multilayer (6 ML) graphitic carbon despite experiencing the same conditions as the on-axis substrates. This optimized graphene growth condition was used for subsequent RE attempts to study the effect of SiC precursor dose, C/Si ratio, and growth rate on epilayer crystallinity and graphene barrier damage. SiC crystalline quality appeared correlated to growth rate, with lower growth rates producing smoother films with fewer polytype inclusions. Single-crystalline, polytype-pure SiC epilayers was achieved on 4° off-axis CVD graphene/4H-SiC(0001). Effects of initial SiC growth parameters on the graphitic carbon release layer were explored via cross-sectional transmission electron microscopy (TEM) and attempts at epilayer transfer. Some growth interfaces exhibited non-uniform multilayer graphitic carbon, motivating further study of this growth system to improve boundary uniformity and SiC epilayer quality.

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9:30am **EM1+AP+CA+CPS+MS+TF-WeM-7 Multiscale Modeling of Self-heating Effects in AlGaN/GaN High Electron Mobility Transistors (HEMT)**, ***Jerry Comanescu,*** National Institute of Standards and Technology*; Albert Davydov,* NIST-Gaithersburg*; Michael Shur,* Theiss Research, Inc.*; Tyler Gervasio, Behrang Hamadani, Michael Lloyd,* NIST-Gaithersburg

AlGaN/GaN based High Electron Mobility Transistors have emerged as state-of-the-art devices in power and RF electronics because of the outstanding electronic properties of the AlGaN/GaN heterostructure. The large breakdown field of GaN (3.3 MV/cm, 11 times higher than silicon) enables HEMT operation in the kV-range while the high mobility of the two-

dimensional electron gas at the AlGaN/GaN interface ensures that HEMTs have a very low on-resistance. In addition, the wide bandgap of GaN makes HEMT devices particularly suitable for high-temperature, high-power, and high-current operations. However, unlike silicon-based devices, the performance of current GaN based devices falls significantly shorter than what is expected based on the outstanding properties of GaN material. This gap in performance is even larger when HEMT devices experience self-heating under high-power operation regime, which strongly affects the device lifetime and reliability. Therefore, understanding the high-temperature operation and the self-heating effect is critical for improving the device design. We report on self-heating effect in AlGaN/GaN HEMTs. We interpret our measurement results using a new compact CAD self-heating model. The model is based on the Unified Charge Control Model (UCCM) and is in excellent agreement with the measured data. Our results allow for the identification of the material properties and device parameters primarily responsible for the temperature dependencies of the device characteristics. The measured temperature dependencies also reveal non-ideal effects related to charge trapping, including threshold voltage instability and current-voltage characteristic hysteresis. The model accounts for the temperature distribution inside the HEMT devices (e.g., distribution of temperature along the channel) which are evaluated by a combination of TCAD simulations, heat transfer finite element simulations, and experiments performed on commercial HEMT devices. The developed compact self-heating model augments TCAD simulations for the Device Technology Co-Optimization approach by linking the AlGaN/GaN HEMT performance and design optimization to material and interface properties.

9:45am **EM1+AP+CA+CPS+MS+TF-WeM-8 Atomic Layer Deposition of High-k Oxide Layers on Aluminum Gallium Nitride: Insight from Time-Resolved Synchrotron Studies***, Nishant Patel, Shreemoyee Chakraborty,* Lund University, Sweden*; Byeongchan So,* lund University, Sweden*; Minho Kim, Alexis Papamichail,* Linkoping University, Sweden*; Rosemary Jones,* Max IV Laboratory, Sweden*; Erik Lind, Vanya Darakchieva,* ***Rainer Timm****,* Lund University, Sweden

Gallium nitride (GaN) and aluminum gallium nitride (AlGaN) are the materials of choice for enabling power electronic devices with superior energy efficiency and very high switching frequency. Such devices are based on metal-oxide-semiconductor (MOS) stacks, where downscaling and leakage control require gate insulators with high dielectric constant, so-called high-k oxides, such as HfO_2. However, device performance and especially switching frequencies are often limited by the low quality of the (Al)GaN/high-k interface. Atomic layer deposition (ALD) is typically used for the synthesis of ultrathin, conformal high-k layers, where the choice of oxide material, ALD parameters, and pre-ALD cleaning methods strongly influence film and interface quality. Many important details about the physics and chemistry of the interface formation still remain unknown. Furthermore, until now all efforts to explore the high-k oxide film formation are based on *ex situ* approaches, meaning that film deposition and characterization of the resulting interface occur in separate steps.

Here, we will present a first time-resolved investigation of the ALD reactions of HfO_2 on (Al)GaN. We have used synchrotron-based ambient-pressure X-ray photoelectron spectroscopy (AP-XPS) and implemented the ALD process in the AP-XPS setup at the MAX IV synchrotron facility. Thus, we succeeded in mapping surface chemistry and electronic properties *in situ* during subsequent ALD half-cycles, which consisted of the deposition of tetrakisdimethylamido-hafnium (TDMA-Hf) and water. We observed a rather inefficient first ALD cycle, compared to other semiconductor ALD reactions, which improved with increasing aluminum content. Thickness and chemical composition of the resulting Hf-oxide film varied significantly if the order of the precursors was changed (TDMA-Hf first or water first). Both observations are against the established ligand-exchange ALD model and highlight the importance of in-depth studies for improving the quality of high-k layers on (Al)GaN.

In addition, we have used XPS to systematically investigate the electronic properties and chemical composition of the interface between different (Al)GaN substrates and HfO_2 or Al_2O_3 high-k oxide films, for different ALD temperatures, where Al_2O_3 layers typically resulted in a more stoichiometric oxide film. The choice of pre-ALD cleaning methods was also found to be of importance, which can enhance ALD efficiency but also result in significant interface contamination. We will discuss how our structural results can be easily implemented to improve device performance.

Electronic Materials and Photonics
Room 207 A W - Session EM2+CA+CPS+MS+SE+TF-WeM
Processing Ultra-Wide Band Gap Ga_2O_3

Moderator: Daniel Pennachio, Naval Research Laboratory

11:00am **EM2+CA+CPS+MS+SE+TF-WeM-13 Ga_2O_3 Polymorphs: Epitaxial Film Growth, Characterization and Contacts***, **Lisa Porter**, Jingyu Tang, Kunyao Jiang, Robert Davis, Posen Tseng, Rachel Kurchin,* Carnegie Mellon University*; Luke Lyle,* Penn State Applied Research Labs*; Carlo Schettini Mejia,* Carnegie Mellon University **INVITED**

The last decade has shown a dramatic increase in research on gallium oxide (Ga_2O_3) as an ultra-wide bandgap semiconductor for electronics that can operate in extreme conditions, such as high power, high temperature and radiation exposure. This presentation will focus on unique and intriguing characteristics associated with two processes that are necessary to produce Ga_2O_3-based devices: the growth of epitaxial films and the formation of ohmic and Schottky contacts. Whereas β-Ga_2O_3 is the thermodynamically stable phase, the other, metastable, phases of Ga_2O_3 can be produced as epitaxial films in either mixed-phase or pure-phase form. Our results, along with those in the literature, indicate that the phase content and other film properties strongly depend on the growth method (e.g., MOCVD, HVPE, mist CVD, etc.) and other conditions during film growth, such as precursor chemistry, flow rates, temperature, and substrate material / orientation. Our group has also conducted comprehensive studies of ohmic and Schottky contacts to β-Ga_2O_3. For reasons that are not well understood, only a few metals have been demonstrated as practical ohmic contacts to Ga_2O_3. Whereas Ti/Au contacts annealed at 400–500 °C are widely used, Cr/Au contacts annealed in a comparable temperature range also form ohmic contacts to Ga_2O_3. Controlled studies of several different elemental-metal Schottky contacts show that their electrical behavior highly depends on the particular Ga_2O_3 surface on which they're deposited; observed behavior ranges from Fermi-level pinning on the (-201) surface to near-ideal Schottky-Mott behavior on the (100) surface. Examples of the phenomena outlined above will be summarized and presented using results from high-resolution transmission electron microscopy, x-ray diffraction, and electrical measurements.

11:30am **EM2+CA+CPS+MS+SE+TF-WeM-15 Compensating Interfacial Parasitic Si Channels in β-Ga2O3 Thin Films Via Fe δ-doping***, **Prescott Evans**, Brenton Noesges, Jian Li, Mark Gordon, Daram Ramdin, Shin Mou, Adam Neal, Thaddeus Asel,* Air Force Research Laboratory, USA

β-Ga_2O_3 is a promising material for high power applications given an ultra-wide bandgap and predicted high break down field. One challenge with β-Ga_2O_3 for lateral device architectures is the presence of undesired Si between epitaxial thin film and substrate which creates a parasitic conduction channel. This channel limits performance and can prevent device modulation. Attempts to remove this interfacial layer using etch methods have proven mostly successful. However, in plasma-assisted oxide molecular beam epitaxy (PAMBE), conventional removal efforts appear unsuccessful. Our results show interfacial Si can reaccumulate at clean β-Ga_2O_3 surfaces from various Si sources inside the MBE tool such as the Si doping effusion cell. Hence, careful growth steps must be considered to avoid Si reaccumulating onto clean β-Ga_2O_3 surfaces in PAMBE. This work presents an alternative to mitigate the influence of this Si parasitic conduction channel via Fe delta doping at the interface. We demonstrate how a thin Fe layer at the interface can compensate interfacial Si and create an interface without excess free charge. The growth methodology presented involves multiple steps to avoid Fe diffusion from the interface. We first deposit the Fe followed by a low temperature (LT) undoped buffer before depositing an Si doped channel layer at higher deposition temperatures. The LT buffer helps minimize Fe surface riding and diffusion while the increased substrate temperature during the Si doped channel improves surface roughness. Secondary ion mass spectrometry (SIMS) results show Fe only resides at the interface between substrate and LT buffer layer with Fe concentration in the LT buffer and Si doped channel below the noise floor of the instrument. Furthermore, SIMS shows a smooth transition in Si concentration from the LT buffer into the intentionally Si-doped channel region avoiding any spikes between the two layers, indicating high degree of controlled doping localization. Initial capacitance-voltage (C-V) measurements on samples with the Fe compensation show no spike in carrier concentration near the substrate interface indicating Fe is fully compensating interfacial Si. These results demonstrate a potential method to mitigate parasitic Si conduction channels in β-Ga_2O_3. However, time-dependent C-V results show there is some capacitance transients when the sample is fully depleted. While Fe

seems initially promising other compensating acceptors such as N or Mg need to be explored given this observation of capacitance transients in Fe-doped structures. Overall mitigating this parasitic interface will help improve yield and performance uniformity in fabricated devices.

11:45am **EM2+CA+CPS+MS+SE+TF-WeM-16 Investigating Metal Gate-Driven Interfacial Reactions in ALD-Grown Al_2O_3 on β-Ga_2O_3**, ***Joy Roy,*** *Adam A. Gruszecki,* The University of Texas at Dallas*; Khushabu S. Agarwal, Paolo La Torraca, Karim Cherkaoui, Paul K. Hurley,* Tyndall National Institute, University College Cork, Ireland*; Chadwin D. Young, Robert M. Wallace,* University of Texas at Dallas

β-Ga_2O_3 is a leading candidate semiconductor for next generation power electronics with the potential to outperform GaN and SiC owing to its high breakdown strength paired with low power losses.[1] Integrating a robust gate dielectric and stable oxide interface is critical in leveraging these properties of β-Ga_2O_3.[2] However, this cannot be achieved without also considering the gate electrodes' reactivity and their influence on oxide properties. This work explores interfacial reactions—particularly those associated with oxygen scavenging—and the resulting variations in gate oxide performance induced by Ni and Ti gate metals in Al_2O_3 on bulk (001) β-Ga_2O_3 substrates.

Interface reactions were analyzed via *in situ* X-ray photoelectron spectroscopy (XPS) in an ultrahigh vacuum (UHV) cluster system. β-Ga_2O_3 samples were scanned as-loaded, after atomic layer deposition (ALD) of ~2 nm Al_2O_3, and a third time following UHV electron beam deposition of Ni or Ti (~1 nm) to assess changes in interface chemistries. Additional chemical states in Ga_2O_3 were below the XPS detection limit after oxide and metal deposition. However, an AlO_x (sub stoichiometric) state appeared in Al core levels (2*p* or 2*s*) after introducing Ti. This, along with a TiO_x state in Ti 2*p*, may imply oxygen scavenging from Al_2O_3. While both metals reacted with surface organic residues from metal-organic precursors, Ti exhibits more carbide formation at the gate/dielectric interface. Additionally, MOSCAPs were fabricated with ~12 nm Al_2O_3 and 10/100 nm of either Ni/Au or Ti/Au as the gate metal for I-V and C-V characterization. Ni/Au devices showed lower frequency dispersion and over two orders of magnitude lower gate leakage in accumulation than Ti/Au samples, consistent with the XPS findings. Dielectric breakdown strength will be further studied to explore electrical stability of the oxides.

In conclusion, a fundamental understanding of gate metals' influence on interface properties is essential for precisely predicting device behavior in power electronics.

This work was supported by the National Science Foundation (Grant ECCS 2154535) at the University of Texas at Dallas and by Research Ireland (Grant 12/US/3755) at Tyndall National Institute through the US-Ireland R&D Partnership. (Corresponding author: Robert M. Wallace.)

[1] S. J. Pearton, F. Ren, M. Tadjer, and J. Kim. J. Appl. Phys. **124**, 220901 (2018).

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Electronic Materials and Photonics

Room 207 A W - Session EM1+AP+CPS+MS+PS+SM+TF-WeA

Materials and Devices in Emerging Memories

Moderators: M. David Henry, Sandia National Labs, **Philip Lee**, University of Kentucky

2:15pm **EM1+AP+CPS+MS+PS+SM+TF-WeA-1 Impact of Precursor Purge Time on the Performance of Ferroelectric Hf0.5Zr0.5O2 Prepared by Plasma-Enhanced Atomic Layer Deposition***, Yong Kyu Choi, Benjamin Aronson, Megan Lenox, Liron Shvilberg,* University of Virginia, USA*; Chuanzhen Zhou,* North Carolina State University*; Kristina Holsgrove,* Queen's University Belfast, UK*; Amit Kumar,* Queen's University Belfast, UK*; Andrea Watson, Stephen J. McDonnell, Jon F. Ihlefeld,* University of Virginia, USA

Hafnium oxide (HfO_2) shows significant potential for non-volatile memory and energy harvesting applications. However, its monoclinic phase lacks polarization, making it unsuitable for ferroelectric applications. Introducing ZrO_2 into HfO_2 (HZO) helps stabilize a ferroelectric phase. Atomic layer deposition (ALD) is the most widely used film processing technique, offering excellent thickness control, conformability, and relatively low processing temperature. Previous research has explored the impact of various metal precursors, oxidizer precursors, and process temperatures on the ferroelectric properties of HZO. One common observation is that the metal precursor purge time has a large effect on the resulting film phase and performance. However, no clear mechanism has been identified to explain this effect. In this presentation, we will discuss how HZO thin film properties change when the metal precursor purge time varies during plasma-enhanced ALD. Reducing the metal precursor purge time from 90 s to 3 s induced a transition from ferroelectric to antiferroelectric properties with double polarization hysteresis loops, higher endurance and polarization stability, and slightly increased in relatively permittivity. Infrared spectroscopy measurements (FTIR-ATR) confirmed that the antiferroelectric properties are due to the antipolar orthorhombic o-I phase, which is consistent with observations from HRTEM and DPC-STEM. The films deposited with shorter purge times showed carbon impurities as identified by ToF-SIMS analysis. This suggests that residual chemical ligands from incomplete precursor removal during the ALD process, in part, stabilizes the antipolar o-I phase. These results show that phase stability in fluorite oxides is influenced by impurities beyond intentional substituents and that stable antiferroelectric responses can be achieved without deliberately altering the material composition, such as adjusting the Hf:Zr ratio to control phase formation.

2:30pm **EM1+AP+CPS+MS+PS+SM+TF-WeA-2 Effect of Atomic Layer Annealing Duration on Phase Stabilization of Hafnium Zirconium Oxide Thin Films***, Nicolas Lam,* University of Virginia*; Gerald Bejger, John Barber,* Virginia Tech*; Megan Lenox, Liron Shvilberg,* University of Virginia*; Christina Rost,* Virginia Tech*; Jon Ihlefeld,* University of Virginia

Significant research has gone into understanding the stabilizing mechanisms and properties of ferroelectric hafnia. This is largely due to its ability to display ferroelectricity in size scales below 10 nm, incorporation in already existing mass production infrastructure, and complementary metal oxide semiconductor compatibility. Today, hafnium zirconium oxide (HZO) is the most studied hafnia alloy due to its low processing temperature. However, the widespread implementation of HZO as a memory material is hindered by a variety of challenges, such as wake–up, imprint, and retention. A major issue is the inability to make phase pure ferroelectric HZO, a metastable non–centrosymmetric polar orthorhombic structure. Commonly cited impurity phases include the metastable tetragonal, antipolar orthorhombic, and equilibrium monoclinic phases. Previous work using the atomic layer annealing (ALA) technique has shown enhanced crystallinity and remanent polarization in pristine HZO films, circumventing significant formation of the antiferroelectric and tetragonal phases. In this work, thin films of HZO were grown using the ALA technique with various ALA treatment durations, ranging from 0 s up to 59 s. Following a deposition of a metal oxide layer using plasma–enhanced atomic layer deposition, the surface of the film was subjected to additional argon plasma. After synthesis and a post–metallization anneal to form the metastable phase, various structural and electrical measurement techniques were used to characterize the films. Grazing-incidence X-ray diffraction shows no formation of the equilibrium monoclinic phase; Fourier transform infrared spectroscopy shows increasing ferroelectric phase concentration with ALA time. Polarization hysteresis measurements show an increasing hysteretic response with ALA time as compared to an antiferroelectric reference sample. Positive up negative down measurements quantified the relative amount of wake–up. The reference devices displayed a 200% increase in remanent polarization while the ALA samples displayed an 8% relative increase with the longest treatment time. The results suggest that ALA can modify the local environment of the deposited films, such that the phase fraction of the ferroelectric phase and the amount of wake–up can be tuned. This results in devices that exhibit minimal to no wake–up. This work furthers the understanding of the effect that ALA has on the resultant film's properties.

2:45pm **EM1+AP+CPS+MS+PS+SM+TF-WeA-3 Understanding Time-Dependent Imprint in Hafnium Zirconium Oxide Based Ferroelectric Tunnel Junctions***, Megan Lenox,* University of Virginia, USA*; Samantha Jaszewski,* Sandia National Laboratories*; Jon Ihlefeld,* University of Virginia, USA*; M. David Henry,* Sandia National Laboratories, USA

While research into understanding the performance-materials property relationship of hafnium zirconium oxide (HZO) based devices has been accelerated in the past decade, their integration into microelectronic products is challenged by their endurance and imprint behavior. Imprint, or a shift in the coercive field following polarization with an initial applied field, lowers HZO remanent polarization (P_r) along the imprint direction, impacting the current transport mechanisms and reducing the overall performance stability when studied in ferroelectric non-volatile memory applications. In these devices, imprint has been hypothesized to result from charge carrier migration at the electrode interface, increasing the charge needed for polarization switching. However, the mechanisms responsible for imprint in ferroelectric tunnel junctions (FTJ) is not understood. To study FTJ imprint phenomena, 7 nm $Hf_{0.7}Zr_{0.3}O_2$ devices with NbN and Nb as the top and bottom electrode, respectively, were fabricated. Polarization-electric field measurements were performed every 2^n seconds, showing a $+V_c$ shift with time.

Resistance measurements, using a pulsing scheme composed of a $\pm V_{max}$ write pulse followed by fifty 0.4 V read pulses at various pulse widths taken every 2^n seconds, showed a drift in the ratio of high and low resistance states, and an overall reduction in the binary state memory window with increasing time, characteristic of imprint. Further, these results highlight imprint impacts on multi-state polarization switching used in neuromorphic memory applications. To investigate imprint mechanisms, pulsed hysteresis measurements taken in 0.1 V intervals followed by a reset pulse at $\pm V_{max}$ showed an 18.1x change in the resistance ratio between the high and low resistance states. However, a similar pulsed hysteresis measurement without the reset pulse had a 11.4x resistance ratio. These results support the generation of time-dependent imprint-free HZO-based FTJs by utilizing selective pulsing schemes, promoting their use in next-generation microelectronics.

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3:00pm **EM1+AP+CPS+MS+PS+SM+TF-WeA-4 Disentangling Gamma-Ray Radiation Effects and Time-Dependent Imprint on Ferroelectric Hafnium Zirconium Oxide-Based Devices***, Samantha Jaszewski,* Sandia National Laboratories*; Megan Lenox, Jon Ihlefeld,* University of Virginia*; M. David Henry,* Sandia National Laboratories

Ferroelectric hafnium oxide (HfO_2) enables technological developments in microelectronics, such as the scaling of ferroelectric random-access memory (FeRAM) and new devices like ferroelectric field-effect transistors (FeFETs) and ferroelectric tunnel junctions (FTJs) that were not previously possible with conventional ferroelectrics. This is due to the material's compatibility with silicon and its ability to exhibit a ferroelectric response in films as thin as 1 nm. Understanding the interaction between radiation and ferroelectric HfO_2-based devices is necessary before these devices can be utilized in radiation-hostile environments. In the literature, it has been reported that gamma-ray radiation can result in a shift of the coercive voltage of ferroelectric HfO_2-based devices, impacting the memory window and, thus, the reliability of these devices. However, ferroelectric HfO_2-based

capacitors have also been shown to exhibit a time-dependent imprint effect in which the coercive voltage shifts over time as a result of the depolarization field in the film, which drives charge redistribution in the ferroelectric layer. As such, it can be challenging to disentangle the effects of gamma-ray radiation and the time-dependent imprint shift when evaluating the performance of these devices.

In this work, ferroelectric hafnium zirconium oxide (HZO) capacitors and ferroelectric tunnel junctions (FTJs) are subjected to 1 and 5 Mrad doses of gamma-ray radiation under grounded and biased conditions. X-ray diffraction and Fourier-transform infrared spectroscopy measurements demonstrate that gamma-ray radiation does not result in phase transformations, further confirmed by capacitance-voltage measurements, which show that the relative permittivity of the HZO capacitors does not change after radiation. Polarization-electric field measurements show shifts in the coercive field after radiation. However, it will be shown that these coercive voltage shifts are due to time-dependent imprint in the material rather than the effects of gamma-ray radiation. This work demonstrates that the structural and electrical properties of ferroelectric HZO-based capacitors and FTJs are not affected by gamma-ray radiation up to doses of 5 Mrad. It also underscores the importance of careful measurement procedures and analysis when evaluating radiation effects in this material.

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Thin Films
Room 206 B W - Session TF+CPS+MS+EM-ThM

Thin Films for Microelectronics I

Moderators: Elton Graugnard, Boise State University, **Robert Grubbs**, IMEC Belgium

8:00am **TF+CPS+MS+EM-ThM-1 Pushing the Limits of Vertical NAND Storage Technology with ALD-based Ferroelectrics**, *Prasanna Venkatesan,* Georgia Institute of Technology*;* ***Asif Khan,*** Georgia Institute of Technology, USA **INVITED**

Solid-state drives (SSDs) continue to serve as the foundation of long-term active data storage in modern data centers. Over the past decade, conventional vertical NAND (vNAND) technology has achieved a remarkable 50× increase in storage density, enabled by advances in physical scaling (x–y and z dimensions) and logic scaling (from multi-level cell, MLC, to quad-level cell, QLC). The explosive growth of artificial intelligence (AI)—with models like GPT-4 surpassing a trillion parameters—has further accelerated the demand for high-capacity, high-performance storage systems to support petabyte-scale datasets.

Today's state-of-the-art vertical NAND devices offer densities nearing 30 Gb/mm^2 with over 300 stacked layers. However, extending this scaling trajectory to 1000 layers and beyond—targeting storage densities exceeding 100 Gb/mm^2—poses significant challenges. Chief among these are reliability concerns intrinsic to charge-trap flash technologies, such as lateral charge migration and the poor endurance of higher logic level operations.

To overcome these limitations, ferroelectric field-effect transistors (FeFETs) have emerged as a promising alternative, enabling further z-direction scaling with improved reliability. This presentation will highlight recent advances in atomic layer deposition (ALD)-based ferroelectric gate stack engineering, and how these innovations can support the development of next-generation NAND architectures capable of 1000-layer integration and ultra-high-density storage.

8:30am **TF+CPS+MS+EM-ThM-3 Electrical Properties of BaTiO3 Thin Films Prepared by Atomic Layer Deposition**, ***Jiayi Chen***, *Asif Khan, Mark Losego,* Georgia Institute of Technology

This talk will discuss our efforts to develop a robust atomic layer deposition process (ALD) to create ferroelectric $BaTiO_3$ thin films. Ferroelectric materials are potential candidates for future low voltage RAM and NAND memory because of their reversible two polarization states under low external electric field. While the CMOS compatible gate dielectric materials HfO_2 and $Hf_{0.5}Zr_{0.5}O_2$ are ferroelectric, they have high coercive fields that make it difficult to lower switching voltages below 1 V. Therefore, perovskite ferroelectric materials, like $BaTiO_3$ are desirable to use for these applications because their coercive voltages can be an order of magnitude lower, approaching 0.1 V. However, these ferroelectric films must be deposited by ALD to match the conformality and small thickness requirements desired for RAM and NAND memory. This talk will present the electrical properties of $BaTiO_3$ thin films deposited by an ALD process using Bis-(1,2,4 triisopropylcyclopentadienyl)-Barium and Titanium Isopropoxide precursors. We are able to achieve dielectric constants as high as 15 in as-grown (non-crystalline) thin films, and 140 in annealed (crystalline) thin films, with low leakage current (10^{-4} A / cm^2 at 3 V). Specifically, we will focus on the variations of dielectric constant and leakage current as we optimize deposition recipe, $BaTiO_3$ thin films' stoichiometry, scale down the thickness from 50 nm to 10 nm, and measure at cryogenic and elevated temperatures. We will also discuss the implications of these measurements, and the possible route to achieve ferroelectric $BaTiO_3$ thin films by ALD.

8:45am **TF+CPS+MS+EM-ThM-4 Interlayer-Modulated Coercive Field in $HfZrO_2$ Ferroelectric Devices**, ***Marshall Frye***[12]*, John Wellington-Johnson, Lance Fernandes, Prasanna Ravindran, Asif Khan, Lauren Garten,* Georgia Institute of Technology

Ferroelectric NAND (FeNAND) using $Hf_{0.5}Zr_{0.5}O_2$ (HZO) offers increased memory density, speed, and decreased operation voltage of NAND compared to charge trap flash technology.[1] However, to compete with charge trap flash, the memory window of FeNAND must be increased above 6 V for 3 bit/cell operation or above 8 V to enable 4 bit/cell operation.[1] Since the memory window is directly related the ferroelectric coercive field (E_c), finding pathways to increase the coercive field of HZO is critical to enable FeNAND. Prior studies show that inserting a dielectric interlayer can increase the coercive field, but the mechanism driving the increase in E_c beyond just adding a capacitor in series is still unclear.[2]

The goal of this work is to test the hypothesis that the increased defect states in the dielectric-HZO interface cause in-built fields that then increase the coercive field.[3] First, we fabricate 19 nm HZO both with and without Al_2O_3interlayers or adjacent layers. Varying the layer thicknesses and positions via atomic layer deposition allows for the determination of how the device structure impacts the ferroelectric switching. Polarization-electric field hysteresis loops and positive-up-negative-down (PUND) show ferroelectric switching for each of the films, with a remnant polarization ($2P_r$) up to 27.4 μC/cm^2. The coercive field increases from 1.01 MV/cm in devices without an additional dielectric layer (19 nm HZO) to 3.11 MV/cm in a 3 nm Al_2O_3 interlayer inserted between two 8 nm layers of HZO (8 nm HZO-3 nm Al_2O_3-8 nm HZO). First-order reversal curve (FORC) analysis reveals an increase in internal bias field in devices with dielectric layers, potentially due to defects at the Al_2O_3 - HZO interface. X-ray photoelectron spectroscopy valence band measurements confirm an increase in mid-gap defect states at this interface compared to bulk of the film. Additionally, temperature-dependent modulus spectroscopy is used to evaluate the activation energy and defect concentration in samples with and without a dielectric layer. These findings provide key insights into mechanisms to modulate coercive field in HZO, enabling the design of FeNAND devices with larger memory windows.

References

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9:00am **TF+CPS+MS+EM-ThM-5 Towards Low-Resistance p-Type Contacts to 2D Transition Metal Dichalcogenides Using Plasma-Enhanced Atomic Layer Deposition**, ***Ageeth Bol,*** University of Michigan, Ann Arbor **INVITED**

One major limitation of 2D transition metal dichalcogenide (TMD) based FETs is the high contact resistance between metallic electrodes and semiconducting channels, particularly for p-type contacts. In this presentation I will address how PEALD of p-type TMDs can be used to improve this contact resistance. First, I will go over controlled doping strategies to form p-type 2D TMD contact materials using PEALD, with an emphasis on Nb Doped WS_2. Our recent results show contact resistancevalues as low as 0.30 ± 0.26 kΩ·μm between Pd and PEALD NbxW1-xS2, demonstrating that low resistance contacts between metal and p-type TMDs are possible. Then, I will discuss reducing unintentional p-doping introduced during PEALD of TMDs. PEALD TMDs typically contain some level of hydrogen impurities that leads to unintentional p-doping. We have shown that these impurities can be reduced by introducing an Ar plasma C step in the standard PEALD TMD process. Finally, the use of remote plasmas in PEALD for contact deposition can lead to the creation of undesired impurities and defects in the 2D TMD channel, possibly impacting electronic behavior. I will present some first insights into the defects that are created during PEALD on 2DTMDs and how we can reduce the number of plasma-induced impurities and defects.

9:30am **TF+CPS+MS+EM-ThM-7 Self-Limiting Atomic Layer Deposition of Few-Layer MoS_2**, ***Sungjoon Kim***, *Jeffrey Elam,* Argonne National Laboratory

Computational energy consumption has been increasing exponentially, making energy-efficient microelectronics and computing an urgent need. Three-dimensional integrated circuits (3D ICs) and neuromorphic computing promise to revolutionize information technology by drastically reducing the energy consumption of computers, and two-dimensional (2D) semiconductors like molybdenum disulfide (MoS_2) can enable such technologies. However, scalable and controllable manufacturing processes are still needed to realize the technology's full potential. Here, we demonstrate the uniform and controlled deposition of few-layered MoS_2 using atomic layer deposition (ALD) for the purposes of memtransistor fabrication. By leveraging the equilibrium shift from material deposition to material etching, a self-limiting deposition of MoS_2 is achieved where material growth is stopped after the initial few layers. The resulting few layer MoS_2 was characterized using Raman spectroscopy and X-ray photoelectron spectroscopy, and was used to fabricate and test memtransistors. This deposition strategy is straightforward, robust and more scalable compared to other methods such as powder CVD and exfoliation.

[1] **AVS Russell and Sigurd Varian Awardee**
[2] **TFD James Harper Award Finalist**

9:45am **TF+CPS+MS+EM-ThM-8 DOE's Energy Efficiency Scaling for Two Decades (EES2): Featuring ALD-Fabricated Microelectronics Devices for Ultra-Energy-Efficient Computation at Argonne National Laboratory**, ***Emilie Lozier,*** U.S. Department of Energy, Advanced Manufacturing Office*; Jeffrey Elam,* Argonne National Laboratory*; Desiree Salazar,* Energetics*; Tina Kaarsberg,* U.S. Department of Energy, Advanced Manufacturing Office

Electricity demand in the U.S. is projected to grow ~2% annually, potentially reaching a 50% increase compared to today by 2050 (International Energy Agency 2025). A major driver of this growth is the rise of energy-intensive AI computation, according to a bottom-up analysis of data center energy use published by Lawrence Berkeley National Laboratory (LBNL) in December 2024. Including cryptocurrency mining, LBNL's report projects that data-center-based computation could account for roughly a quarter of total U.S. electricity consumption by 2028. While efforts are underway to increase generation to the grid, any solution must simultaneously address the energy efficiency of compute if it is to be successful. Kicking off three years ago, the U.S. Department of Energy (DOE) Advanced Materials and Manufacturing Technologies Office (AMMTO) has already been leading a multi-organization effort united around the shared aim of advancing ultra-energy-efficient compute technologies. This collaborative effort, known as the Energy Efficiency Scaling for Two Decades (EES2) initiative, is uniquely situated to take on this energy challenge. Through EES2, DOE/AMMTO has convened eight working groups representing more than 70 voluntarily pledging organizations across industry, academia, nonprofits and the National Labs to draft an R&D Roadmap describing technologies-to-beat to achieve biennial energy efficiency doubling for the compute stack compounding to a 1,000X efficiency increase by 2040. Moreover, Version 1.0 of the R&D Roadmap (available here: https://eere-exchange.energy.gov/FileContent.aspx?FileID=f4234e29-cc0c-4a56-a510-86b616ab5535) has spurred a suite of EES2-identified and DOE-funded research projects to pursue some of the most promising technologies for enabling ultra-energy-efficient computation. This presentation will highlight one such project at Argonne National Laboratory – with collaborators at Stanford University, Northwestern University, and Boise State University – that has been advancing two-dimensional semiconductor field-effect transistors (2D-FETs) and memtransistors, both fabricated with atomic layer deposited (ALD) molybdenum sulfide (MoS_2) with potential to achieve 50X and 10,000X energy efficiency improvements, respectively. Along with timely project updates, this presentation will also discuss how the Argonne project will integrate with the finalized Version 1.0 of the EES2 R&D Roadmap, that is due to be published in the second half of 2025.

11:00am **TF+CPS+MS+EM-ThM-13 Integrated Magnetoacoustic Isolator with Giant Non-Reciprocity**, *Bin Luo, Benyamin Davaji,* ***Nian-Xiang Sun,*** Department of Electrical and Computer Engineering, Northeastern University **INVITED**

Recent advances in integrated nonreciprocal components—such as isolators and circulators—have enabled transformative wireless communication and sensing technologies, including full-duplex radio, in-band self-interference cancellation, and protected high-power transmission systems. While commercial ferrite-based isolators offer low insertion loss and high power handling, their reliance on kOe-level bias fields, high-temperature ferrite growth, and bulky permanent magnets severely limits their compatibility with CMOS processes and low-power applications.

To address these limitations, magnetoacoustic isolators have emerged as a promising class of passive, CMOS-compatible, and power-efficient nonreciprocal devices. These isolators consist of magnetic heterostructures integrated within the propagation path of surface acoustic waves (SAWs) on piezoelectric substrates. Magnetoelastic and magnetorotational coupling mechanisms enable strong spin wave–acoustic wave interactions, generating hybrid magnetoacoustic waves with dramatically asymmetric damping rates in opposite directions. This asymmetry yields unidirectional transmission, fundamental to nonreciprocal operation.

Despite progress, early devices suffered from weak non-reciprocity, primarily due to a mere helicity mismatch effect and an inherent symmetric spin wave dispersive relation in single-layer magnetic films. Recent efforts have focused on engineering magnetic stacks with nonreciprocal spin wave dispersion. Key examples include: (i) **interfacial Dzyaloshinskii–Moriya interaction (iDMI) stacks** like CoFeB/Pt, (ii) **interlayer dipolar-coupled (IDC) stacks** such as FeGaB/SiO_2/FeGaB, and (iii) **RKKY synthetic antiferromagnets** like CoFeB/Ru/CoFeB. These architectures achieve nonreciprocity strengths up to 250 dB/mm. Recent demonstrations using shear-horizontal waves in $LiTaO_3$ substrates coupled to ferromagnetic and anti-magnetostrictive bilayers have yielded nonreciprocity levels of 60–82 dB/mm with simpler fabrication.

Nevertheless, a persistent challenge remains in reducing insertion loss while maintaining wide bandwidth and high isolation. We will introduce our recent efforts in a **fundamental mode SAW-driven** magnetoacoustic isolator with **giant non-reciprocity** and a **wideband nonreciprocal** magnetoacoustic isolator based on **non-collinear dipolar-coupled ferromagnetic stacks**. The talk will provide a comprehensive overview of the mechanisms, material platforms, and experimental breakthroughs driving the field of magnetoacoustic isolators. We will highlight the path toward integrated, low-loss, and high-performance nonreciprocal components for future quantum, RF, and IoT systems.

11:30am **TF+CPS+MS+EM-ThM-15 Stress Control and Thermal Stability of a FeCo-Ag Multilayer Thin Films for Use in Magnetoelectric Heterostructures**, ***Thomas Mion,*** *Konrad Bussmann,* US Naval Research Laboratory

This investigation studies the stress control and thermal properties of FeCo/Ag multilayer thin films prepared by sputter deposition for their potential applications in magnetoelectric heterostructure devices. While development of magnetoelectric devices has increased, the practical implementation of magnetic thin films is often confounded by additional processing and packaging steps which can be detrimental to the quality of the magnetic film and subsequently the performance of the device. We show the annealing of the FeCo/Ag multilayers is robust until annealing temperatures reach 300 – 400 C where a breakdown of the Ag leads to an increased coercive field, and annealing >400 C is severely detrimental to the soft magnetism of the system as the Ag layers deteriorate. Additionally, as-deposited stress can play a dominant role in micromechanical devices when released. We will show the stress control of this ferromagnetic thin film through in-situ substrate bias allows the films to be tailored from a broad range of +320 MPa tensile to -300 MPa compressive with application of up to a -120 VDC bias during deposition.

11:45am **TF+CPS+MS+EM-ThM-16 Extraordinary Magnetoresistance in High-Mobility $SrTiO_3$ Thin Films**, ***Zhifei Yang***[1]*, Shivasheesh Varshney,* University of Minnesota*; Sreejith Sasi Kumar, Tristan Steegemans, Rasmus Bjørk, Dennis Valbjørn Christensen,* Technical University of Denmark*; Bharat Jalan,* University of Minnesota

Magnetoresistive sensors are widely used to detect magnetic fields by measuring changes in electrical resistance. One such effect, extraordinary magnetoresistance (EMR), arises from the geometry of semiconductor-metal hybrid structures that combine high-mobility semiconductors with highly conductive metals. EMR strongly depends on both the semiconductor's mobility and the quality of the metal-semiconductor contact (ohmic contact with low contact resistance). The device geometry further influences boundary conditions and current paths under magnetic fields, enabling flexible design and performance tuning. While most previous EMR studies have focused on III-V semiconductors and 2D materials, there has been limited exploration of oxide-based systems.

Here, we demonstrate EMR in high-quality La-doped $SrTiO_3$ thin films grown on $SrTiO_3$ (001) substrates using hybrid molecular beam epitaxy (MBE). We grow films with carrier concentrations ranging from ~2×10^{17} cm^{-3} to ~1×10^{20} cm^{-3}, achieving Hall mobilities from ~300 $cm^2/(V\cdot s)$ up to over 50,000 $cm^2/(V\cdot s)$ at 1.8 K. Using an asymmetric device geometry that breaks mirror symmetry between voltage probes, we observe corresponding asymmetry in magnetoresistance (MR) measurements. With embedded metals that are ohmic contacts to $SrTiO_3$, we achieve an MR ((R(B) – R(0))/R(0), where R(B) is the measured resistance at magnetic field B) approaching 9000% at 9 T and 1.8 K, which is over 3900% higher than the intrinsic MR of $SrTiO_3$ – a *world record* for an oxide-based EMR device! Finite element simulations of current flow and MR in these $SrTiO_3$-based hybrid structures align well with experimental data, validating the design principles. These results establish the potential of complex oxide systems for low-temperature EMR sensors and open opportunities for integrating oxide heterostructures in future magnetoelectronic devices. In this presentation, we will discuss the hybrid MBE growth and microfabrication of high-mobility $SrTiO_3$ thin films, along with device optimization strategies and detailed magnetotransport measurements across various temperature and magnetic field ranges.

[1] **AVS Graduate Research Awardee**

12:00pm **TF+CPS+MS+EM-ThM-17 Examining the Spin Structure of Altermagnet MnTe Epilayers Grown by Molecular Beam Epitaxy**, ***Qihua Zhang***[1], The Pennsylvania State University; *Mingyu Yu,* University of Delaware; *Alexander Grutter, Christopher Jenson, William Ratcliff, Julie Brochers,* National Institute for Science and Technology (NIST); *Narendirakumar Narayanan, Thomas Heitmann,* University of Missouri; *Nitin Samarth, Stephanie Law,* The Pennsylvania State University

As a new class of magnetic materials, altermagnets feature alternating arrangement of magnetic moments with zero net magnetization, a typical characteristic of an antiferromagnet; yet they also feature large spin splitting in its electronic band structure. NiAs-phase (α-) MnTe has gained significant attention as a candidate of altermagnet family owing to its large spin-splitting energy and high transition temperature. In this study, we investigate the altermagnet properties of MBE-grown α-MnTe layers using neutron diffraction experiments. We first study and optimize the growth conditions of MnTe layers grown directly on InP (111)A substrates. It is seen that using a lower growth temperature result in a narrower full-width-at-half-maximum (FWHM) in the x-ray diffraction (XRD) rocking curves, but will introduce whiskers on the surface, while increasing the Te/Mn flux ratio improves both the crystalline quality and the surface morphology. With a temperature window of 250-400 °C and a Te/Mn flux ratio of 3, we further obtain high quality α-MnTe films with a 0.8 nm surface roughness and a corresponding threading dislocation density of ~7.5×10^{8} cm^{-2}. Temperature-dependent neutron diffraction measurements were performed on the MnTe films grown with optimized conditions. A fitted Néel temperature of 304 K was obtained based on the half-order antiferromagnetic peak along the (0001) direction, which confirmed the bulk-like antiferromagnetic behavior in the α-MnTe. Using polarized neutron reflectometry, substantial spin asymmetry is captured while very small net magnetization (up to 4 emu/cm^3) across the MnTe layer is obtained, highlighting a near-to-ideal stoichiometric α-MnTe. Angle-resolved photoemission spectroscopy is further used to confirm the spin splitting in the eletronic band structure. This study carefully clarifies the magnetic band structure in a promising altermagnet candidate and introduces potential methods of controlling the ferromagnetism in the materials.

[1] **TFD Distinguished Technologist Award**

Thin Films
Room 206 B W - Session TF+CPS+MS+EM-ThA

Thin Films for Microelectronics II

Moderators: Lauren Garten, Georgia Institute of Technology, **Christophe Vallee**, University at Albany

2:15pm **TF+CPS+MS+EM-ThA-1 Area Selective Deposition Processing in the Memory Industry: How to Take Advantage of the High-Volume Manufacturing Environment**, ***Francois Fabreguette***, *Jeff Hull, Huicheng Chang, Erik Byers, Gurtej Sandhu,* Micron Technology **INVITED**

Aggressive scaling from node to node in the memory industry has led to a paradigm shift towards Area Selective Deposition (ASD) technique to overcome traditional processing challenges. For example, punches or etches not being capable anymore in High Aspect Ratio structures >100:1 can be replaced by selective deposition processes on the sidewall only, eliminating the need to clear a bottom contact. Likewise, ASD can be used to heal a contact seam that can easily form when the deposited metal pinches off at the top of a High-Aspect ratio structure, leavinga void in the middle of the filled contact. Finally, in tiered structures used for 3D memory scaling, ASD allows for dielectric re-deposition on one tier type selective to the other tier type for cell sculpting without any critical dimension penalty.The present abstract covers a few examples of ASD processes developed in Micron High Volume Manufacturing environment:The state-of-the-art 300mm wafer tooling capability as well as multiple full-wafer inline metrology techniques (such as X-Ray fluorescence, X-ray Photoelectron Spectroscopy, X-Ray Reflectivity, Ellipsometry, Atomic Force Microscopy) allows to characterize the loss of selectivity on the non-growth surfaces on wafer-level. This provides across-wafer inhibition efficiency, which is criticalfor Area Selective Deposition future adoption in large scale production. The case study of ASD TiN using new high-temperature oxide inhibitors is presented. The systematic inline metrology characterization of the inhibited blanket oxide surfaces after TiN deposition at various temperatures is used to determine the best selectivity conditions as well as individual inhibitor performance benchmarked to the best-known oxide inhibitor typically used in the ASD community. Besides, Fourier Transform Infrared (FTIR) spectroscopy, Water Contact Angle measurements (WCA) and carbon content from XPS measurements were performed immediately after inhibition. Theyprovided the surface signature of each inhibitor and were correlated to their overall inhibition efficiency.

2:45pm **TF+CPS+MS+EM-ThA-3 BEOL-compatible (≤300 °C) top-gate HfO_2/ZnSnO Transistors Enabled by Atomic Layer Deposition for Advanced Memory Integration**, ***Changyu Park***, *Jinsung Park, Joohee Oh, Hyoungsub Kim,* Sungkyunkwan University, Republic of Korea

Amorphous oxide semiconductors (AOSs) are promising channel materials for three-dimensional (3D) dynamic random-access memories (DRAMs) owing to their structural uniformity from a stable amorphous phase, low-temperature processability, and extremely low off-state current enabled by their wide bandgap [1]. Atomic layer deposition (ALD) further enhances their applicability by offering conformal coverage in high-aspect-ratio structures and high film quality at low processing temperatures. Among the various AOSs, zinc tin oxide (ZTO) is particularly attractive due to its efficient carrier transport, facile composition tunability, reliance on earth-abundant elements, and high thermal stability [2]. For back-end-of-line (BEOL) integration in 3D DRAM, ZTO must be combined with ALD-grown high-κ dielectrics in top-gate architectures; however, most previous studies have primarily focused on bottom-gate thin-film transistors (TFTs) [3,4].

In this work, we demonstrate the fabrication and characterization of top-gate TFTs with ZTO channels and HfO_2 gate dielectrics, both integrated via ALD at temperatures up to300 °C for BEOL-compatible processing. Guided by the ALD growth behavior of ZnO and SnO_2, ZTO films with various compositions were deposited using a super-cycle method with diethylzinc (DEZ) and tetrakis(dimethylamino)tin(Ⅳ) (TDMASn) at 250 °C, employing ozone (O_3) as the oxidant. After annealing of the ZTO channel at 300 °C for 1 h in ambient air, indium tin oxide source/drain electrodes were formed. The HfO_2 gate dielectric was subsequently deposited via ALD using O_3 at 230 °C.The extracted average parameters of top-gate TFTs with an optimized ZTO composition confirmed their suitability for DRAM cell operation, exhibiting a threshold voltage (V_{th}) of 0.15V, a saturation mobility of 4.3cm^2/V·s, a subthreshold swing of 76mV/dec, and an on/off current ratio exceeding 10^7. Device reliability was further evaluated through positive and negative bias stress tests at ±3 MV/cm, resulting in V_{th} shifts of +0.47 V and –0.12 V, respectively, which are comparable to recent reports on bottom-gate device configuration [3].

[1] A.R. Choi *et al.*, Chem. Mater. **36**, 2194 (2024)

[2] B. Lu *et al.*, Curr. Opin. Solid State Mater. Sci. **27**, 101092 (2023)

[3] J. Choi. *et al.*, ACS Appl. Electron. Mater. **7**, 215 (2025)

[4] J.S. Hur *et al.*, Nanoscale Horiz. **9**, 934 (2024)

3:00pm **TF+CPS+MS+EM-ThA-4 Photoluminescence Spectroscopy of Ultra-Thin GeSn Alloys Grown on Ge-on-Si Substrates**, ***Vijay Gregory***, *Lia Guo, Jay Mathews,* University of North Carolina at Charlotte

Silicon (Si) based devices have dominated the electronics industry over the past decades but are not suitable for making lasers due to their optical properties. As an indirect bandgap semiconductor, Si has inefficient optical emission and therefore cannot be used to make a light source on a Si chip. As an alternative, germanium (Ge), incorporated with tin (Sn), can be grown on Si and is currently being used for photonic devices. GeSn exhibits direct bandgap emission at room temperature and is ideal for an on Si light source. However, they suffer from low intensity due to high defect densities which cause nonradiative recombination.

In this work, we study GeSn/Ge/Si samples with varying percentages of Sn. The materials were grown with sub 100 nm thickness resulting in fully strained thin films which reduce the dislocations caused by lattice relaxation. The emission spectrums of these ultra-thin layers were measured using photoluminescence (PL) spectroscopy to probe the quality of the materials as on Si light sources.

3:15pm **TF+CPS+MS+EM-ThA-5 Highly Ordered NiO (111) Films on Sapphire Substrates via Low-Temperature Hollow Cathode Plasma-ALD and Their Post-Deposition Annealing Characteristics**, *Fatih Bayansal, Steven Allaby, Habeeb Mousa, Helena Silva,* ***Necmi Biyikli***, University of Connecticut

Nickel oxide (NiO) is a promising p-type wide band gap semiconductor material for next generation optoelectronic and energy devices. In this study, the growth process and thermal annealing behavior of NiO thin films grown on c-plane sapphire substrates by hollow-cathode plasma-assisted atomic layer deposition (HCP-ALD) method were investigated. $NiCp_2$ was used as the nickel precursor heated at 100°C, and O_2 plasma was preferred as the oxidizing agent under 100W rf-power and 20 sccm flow rate. The films were grown within a substrate temperature range of 100 – 250°C.

The obtained film samples showed high transmittance in the visible spectrum and exhibited strong absorption in the UV spectrum. Optical band gap values determined by Tauc analysis were found between 3.54 and 3.59eV. The refractive indices increased with the growth temperature and reached 2.38, while the extinction coefficient and film porosity decreased for higher temperature films. X-ray diffraction (XRD) analyses revealed that the films exhibit a highly textured structure with exclusive (111) orientation. No peaks belonging to any other phase or crystal plane were observed. Moreover, grazing incidence XRD (GIXRD) measurements showed no detectable peaks, confirming the monocrystalline film character, and suggesting a surface-parallel alignment and potentially dense and thin film morphology. In addition, shifts in the diffraction peaks were observed depending on the growth temperature.

In order to evaluate the thermal stability and performance of the films, the samples grown at 250°C were annealed at 300, 350 and 400°C. Ongoing studies include characterization of electrical properties (Hall effect) such as carrier density, mobility and conduction type as well as crystal structure (XRD, TEM) and chemical composition (XPS). This holistic approach will contribute to understanding the impact of post-deposition annealing on the crystal quality and charge transport properties of NiO films.

This work contributes to the development of optimized p-type oxide semiconductors for transparent electronics and heterojunction-based devices through controlled low-temperature ALD process and post-deposition thermal engineering.

3:30pm **TF+CPS+MS+EM-ThA-6 Textured Growth and Electrical Characterization of Zinc Sulfide on Back-End-of-the-Line (BEOL) Compatible Substrates**, ***Claire Wu***, *Mythili Surendran, Anika Priyoti, Gokul Anilkumar,* University of Southern California*; Chun-Chen Wang,* Taiwan semiconductor Manufacturing Company, Taiwan*; Cheng-Chen Kuo, Cheng-Hsien Wu,* Taiwan Semiconductor Manufacturing Company, Taiwan*; Rehan Kapadia,* University of Southern California*; Xinyu Bao,* Taiwan Semiconductor Manufacturing Company, Taiwan*; Jayakanth Ravichandran,* University of Southern California

Scaling of transistors has enabled continuous improvement in the performance of logic devices, especially with recent advances in materials engineering for transistors. However, there is a need to surpass the horizontal limitations in chip manufacturing and incorporate the vertical or third dimension. To enable monolithic three-dimensional (M3D) integration of high-performance logic, one needs to solve the fundamental challenge of low temperature (<450 °C) synthesis of high mobility n-type and p-type semiconductor thin films that can be utilized for fabrication of back-end-of-line (BEOL) compatible transistors.1 Transition metal oxides are promising n-type materials; however there is a lack of p-type materials that can meet the stringent synthesis conditions of BEOL manufacturing. Zinc sulfide (ZnS), a transparent wide band-gap semiconductor, has shown room temperature p-type conductivity when doped with copper2 and crystallizes below 400oC when grown by pulsed laser deposition (PLD).3 Here, we report growth of crystalline thin films of ZnS by PLD on a variety of amorphous and polycrystalline surfaces such as silicon nitride, (SixNy) thermal silicon dioxide, (SiO2), hafnium dioxide, (HfO2), yttrium oxide (Y2O3), platinum, sapphire (Al2O3), and titanium nitride (TiN). X-ray diffraction shows texturing of ZnS on all surfaces, including when ZnS is directly grown on HF buffered oxide etched silicon. Crystalline quality is investigated using grazing incidence wide angle X-ray scattering measurements. Surface and interface quality is measured using X-ray reflectivity and atomic force microscopy measurements. Electrical characterization of the ZnS films is done by J-V measurements of ZnS on platinum and metal-oxide-semiconductor capacitor (MOSCAP) measurements of ZnS on SiO2 on heavily doped silicon. The J-V measurements indicate low leakage current on the order of 10-8 A/cm-2 with electric field of 0.013 MV/cm2 and the MOSCAP characteristics show bilayer capacitor behavior, which points to ZnS being highly intrinsic with very low unintentional, electrically active point defects. Further work on doping ZnS with copper or other p-type candidate dopants are needed to demonstrate ZnS as a dopable wide band gap semiconductor for channels compatible with BEOL manufacturing. This work showcases the capability of novel thin film growth technique of a wide band-gap sulfide semiconductor in BEOL compatible conditions with potential for technological applications in transistor manufacturing.

1. S. Datta et al., IEEE Micro.39, 6, 8-15 (2019)

2.R. Woods-Robinson et al., Adv. Electron. Mater. 2, 1500396 (2016)

3. M. Surendran et al., Adv. Mater. 36, 2312620 (2024)

3:45pm **TF+CPS+MS+EM-ThA-7 Thermal Atomic Layer Deposition of Molybdenum Phosphide Films**, *John D. Hues, Wesley Jen,* ***Nolan Olaso****, Steven M. Hues, Elton Graugnard,* Boise State University

Aggressive scaling of semiconductor technology nodes has led to copper-based interconnects beginning to approach the maximum scaling limit of the material, beyond which unacceptably high increases in interconnect resistance due to electron scattering at grain boundaries and interfaces begins to cause degradation of device performance. New materials are required for interconnect applications beyond the 7 nm node to produce devices with acceptable signal delay and power consumption parameters. Topological semimetals are one family of materials that are of interest for the replacement of copper in interconnect applications due to the predicted favorable resistance scaling, which results from topologically protected surface states that suppress electron scattering and act as conduction pathways in nanoscale films. This decrease in interconnect resistance has the potential to improve the efficiency of integrated circuits through reduced RC delay and reduced energy consumption, which is under increased scrutiny due to increasing computing demands, such as generative artificial intelligence and cloud computing. In order to aid in the integration of these promising materials into production environments, scalable synthesis methods, such as atomic layer deposition (ALD), are needed. In addition to the development of deposition chemistries for these materials, insight into how processing conditions impact the performance of the resulting film are also of importance. Here, we report on a new thermal ALD deposition chemistry for molybdenum phosphide (MoP) using molybdenum(V) chloride ($MoCl_5$) and tris(dimethylamino)phosphine (TDMAP) at temperatures between 350 °C and 425 °C. In-situ and ex-situ characterization of the resulting films was performed using quartz crystal microbalance (QCM), x-ray photoelectron spectroscopy (XPS), x-ray diffraction (XRD), atomic force microscopy (AFM), scanning electron microscopy (SEM), and four-point probe measurements. QCM measurements demonstrated a linear mass increase of 164 ng/cycle at 375 °C. Film deposition was confirmed through XRD and XPS chemical state analysis. The resulting films were near stoichiometric as determined via XPS. AFM and SEM characterization revealed a polycrystalline morphology with nanoscale grain sizes. Four-point probe measurements of the as-deposited films indicated non-ideal electrical performance which was subsequently improved through post deposition annealing. Although more work is needed to improve electrical performance, this new ALD chemistry may provide a method for the deposition of MoP films at the dimensions required for next generation technology nodes.

CHIPS Act : Semiconductor Manufacturing Science and Technologies

Room Ballroom BC - Session CPS+MS-ThP

CHIPS Act: Semiconductor Manufacturing Science and Technologies Poster Session

CPS+MS-ThP-2 Nanostructural Characterization of 3D DRAM by 3D Reconstruction*, Wenbin Fan,* Applied Materials

As the continuous scaling of Dynamic Random Access Memory (DRAM) technology, semiconductor industry is evolving from two-dimensional (2D) to three-dimensional (3D) DRAM to provide the massive amounts of memory required for AI applications. 3D DRAM is expected to require advanced processes (deposition, etching and doping capabilities) to shape and form increasingly precise 3D structures across a 300mm wafer. In this work, a methodology for characterizing the nano structure of 3D DRAM to optimize these various processes is introduced as a promising solution to overcome current metrology limitation in semiconductor industry. Virtually reconstruction of 3D DRAM by hundreds of 2D Scanning Electron Microscopy (SEM) images is successfully demonstrated, offering superior detailed 3D nanostructure and extending the traditional SEM or Transmission Electron Microscopy (TEM) capability. Quantitative analysis on the reconstructed 50-pair Si/SiGe multilayers 3D DRAM is presented with excellent results in the measurements of 2D/3D Critical Dimension (CD) and defectivity.

CPS+MS-ThP-3 Summer Program Advancing Robotics and Knowledge in Microelectronics for K-12 (SPARK)*, Parmida Amngostar, Soheyl Faghir Hagh, Alireza Fath, Yi Liu, Ian Cassidy, Swarup Chakraborty, Alexander Hoefer, Lanhjamin Tran, Cooper Duggan, Dryver Huston,* ***Jackson Anderson****, Tian Xia,* University of Vermont

Since global trade disruption highlighted supply chain vulnerabilities, domestic semiconductor manufacturing has emerged as a national priority, as evidenced through passage of the CHIPS and Science Act in 2022. With this boost in spending comes the risk of workforce shortages, with as many as 58% of new jobs at risk of being unfilled [1]. In Vermont, IBM Microelectronics (now GlobalFoundries) have had a continuous presence since 1957, creating a robust ecosystem of semiconductor manufacturing and design expertise, however local workforce challenges remain. While Vermont has a 91.2% high school completion rate, only 57% of those age 18-24 go on to attend an institution of higher education [2]. Traditionally, microelectronics and semiconductor concepts are not covered in the K-12 curriculum, leaving nearly half the population underinformed about a vital employment industry.

In this work we bridge the microelectronics education gap in Vermont through a workshop developed to educate K-12 science teachers, enabling them to more confidently introduce concepts in the classroom and informal settings. The developed workshop was run for the first time in June of 2025 and covered topics such as electrical prototyping, board and integrated circuit design, programming microcontrollers, interfacing with sensors, microelectronics fabrication, and advanced robotics. Activities were developed such that they could be run in a K-12 setting using the kits provided to teachers during the workshop. Materials have been published at the program website for free use [3]. The initial cohort consisted of 13 teachers from across the state whose instructional focus varied from 4th through 12th grade. Feedback from the attendees will be presented, along with learnings and considerations for any others hoping to offer a workshop like this in their jurisdiction.

[1] “Chipping Away” Report, Semiconductor Industry Association. July 2023.

[2] American Community Survey Table S1501, 2023 5-yr estimates. https://data.census.gov/table/ACSST5Y2023.S1501?g=040XX00US50. Accessed 08/2025.

[3] UVM SPARK. https://sites.google.com/view/spark-vtk12/home. Accessed 08/2025

This work was supported by NSF grant No. 2119485 and the V-GaN Tech Hub.

CPS+MS-ThP-4 Ge and Gesn Photodetectors for Infrared Application: Toward Si-Compatible High Responsivity Devices.*, Q.M. Kamrunnahar,* *Yining Liu, Jay Mathews,* University of North Carolina at Charlotte

Silicon photodetectors are crucial for current optoelectronics due to their CMOS compatibility, scalability, and low fabrication cost. Si is suitable for various applications, from imaging to on-chip optical interconnects, for these features. But the native absorption edge at ~1.1 µm has limited the application of Si in the telecom and critical infrared (IR) communication windows. This shortcoming has created the necessity for advanced materials that can extend detection beyond the range of silicon while remaining compatible with large-scale integration. In this case, Germanium (Ge) is a suitable option with its strong absorption up to ~1.55 µm. It has emerged as one of the most promising and widely used materials for telecom-band photonics and electronics. Recently, GeSn has shown its potential at the extended range of 2.5 to 3 µm. The behavior of Ge can be gained as a direct bandgap by adding tin (Sn). Thus, Ge and GeSn-based photodetectors could be strong candidates in the IR region and can replace the highly expensive InGaAs or HgCdTe photodetectors. In this work, we are presenting our current project to fabricate Ge and GeSn based photodetectors which can work in the infrared region. We have successfully fabricated initial devices using standard microfabrication techniques (Photolithography, etching, ebeam evaporation and lift off) and still working to improve the responsivity and detectivity of the photodetectors which is comparable with industry.

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