Thin Films
Room 206 B W - Session TF+CPS+MS+EM-ThA

Thin Films for Microelectronics II

Moderators: Lauren Garten, Georgia Institute of Technology, **Christophe Vallee**, University at Albany

2:15pm **TF+CPS+MS+EM-ThA-1 Area Selective Deposition Processing in the Memory Industry: How to Take Advantage of the High-Volume Manufacturing Environment**, ***Francois Fabreguette***, *Jeff Hull, Huicheng Chang, Erik Byers, Gurtej Sandhu,* Micron Technology **INVITED**

Aggressive scaling from node to node in the memory industry has led to a paradigm shift towards Area Selective Deposition (ASD) technique to overcome traditional processing challenges. For example, punches or etches not being capable anymore in High Aspect Ratio structures >100:1 can be replaced by selective deposition processes on the sidewall only, eliminating the need to clear a bottom contact. Likewise, ASD can be used to heal a contact seam that can easily form when the deposited metal pinches off at the top of a High-Aspect ratio structure, leavinga void in the middle of the filled contact. Finally, in tiered structures used for 3D memory scaling, ASD allows for dielectric re-deposition on one tier type selective to the other tier type for cell sculpting without any critical dimension penalty.The present abstract covers a few examples of ASD processes developed in Micron High Volume Manufacturing environment:The state-of-the-art 300mm wafer tooling capability as well as multiple full-wafer inline metrology techniques (such as X-Ray fluorescence, X-ray Photoelectron Spectroscopy, X-Ray Reflectivity, Ellipsometry, Atomic Force Microscopy) allows to characterize the loss of selectivity on the non-growth surfaces on wafer-level. This provides across-wafer inhibition efficiency, which is criticalfor Area Selective Deposition future adoption in large scale production. The case study of ASD TiN using new high-temperature oxide inhibitors is presented. The systematic inline metrology characterization of the inhibited blanket oxide surfaces after TiN deposition at various temperatures is used to determine the best selectivity conditions as well as individual inhibitor performance benchmarked to the best-known oxide inhibitor typically used in the ASD community. Besides, Fourier Transform Infrared (FTIR) spectroscopy, Water Contact Angle measurements (WCA) and carbon content from XPS measurements were performed immediately after inhibition. Theyprovided the surface signature of each inhibitor and were correlated to their overall inhibition efficiency.

2:45pm **TF+CPS+MS+EM-ThA-3 BEOL-compatible (≤300 °C) top-gate HfO_2/ZnSnO Transistors Enabled by Atomic Layer Deposition for Advanced Memory Integration**, ***Changyu Park***, *Jinsung Park, Joohee Oh, Hyoungsub Kim,* Sungkyunkwan University, Republic of Korea

Amorphous oxide semiconductors (AOSs) are promising channel materials for three-dimensional (3D) dynamic random-access memories (DRAMs) owing to their structural uniformity from a stable amorphous phase, low-temperature processability, and extremely low off-state current enabled by their wide bandgap [1]. Atomic layer deposition (ALD) further enhances their applicability by offering conformal coverage in high-aspect-ratio structures and high film quality at low processing temperatures. Among the various AOSs, zinc tin oxide (ZTO) is particularly attractive due to its efficient carrier transport, facile composition tunability, reliance on earth-abundant elements, and high thermal stability [2]. For back-end-of-line (BEOL) integration in 3D DRAM, ZTO must be combined with ALD-grown high-κ dielectrics in top-gate architectures; however, most previous studies have primarily focused on bottom-gate thin-film transistors (TFTs) [3,4].

In this work, we demonstrate the fabrication and characterization of top-gate TFTs with ZTO channels and HfO_2 gate dielectrics, both integrated via ALD at temperatures up to300 °C for BEOL-compatible processing. Guided by the ALD growth behavior of ZnO and SnO_2, ZTO films with various compositions were deposited using a super-cycle method with diethylzinc (DEZ) and tetrakis(dimethylamino)tin(Ⅳ) (TDMASn) at 250 °C, employing ozone (O_3) as the oxidant. After annealing of the ZTO channel at 300 °C for 1 h in ambient air, indium tin oxide source/drain electrodes were formed. The HfO_2 gate dielectric was subsequently deposited via ALD using O_3 at 230 °C.The extracted average parameters of top-gate TFTs with an optimized ZTO composition confirmed their suitability for DRAM cell operation, exhibiting a threshold voltage (V_{th}) of 0.15V, a saturation mobility of 4.3cm^2/V·s, a subthreshold swing of 76mV/dec, and an on/off current ratio exceeding 10^7. Device reliability was further evaluated through positive and negative bias stress tests at ±3 MV/cm, resulting in V_{th} shifts of +0.47 V and –0.12 V, respectively, which are comparable to recent reports on bottom-gate device configuration [3].

[1] A.R. Choi *et al.*, Chem. Mater. **36**, 2194 (2024)

[2] B. Lu *et al.*, Curr. Opin. Solid State Mater. Sci. **27**, 101092 (2023)

[3] J. Choi. *et al.*, ACS Appl. Electron. Mater. **7**, 215 (2025)

[4] J.S. Hur *et al.*, Nanoscale Horiz. **9**, 934 (2024)

3:00pm **TF+CPS+MS+EM-ThA-4 Photoluminescence Spectroscopy of Ultra-Thin GeSn Alloys Grown on Ge-on-Si Substrates**, ***Vijay Gregory***, *Lia Guo, Jay Mathews,* University of North Carolina at Charlotte

Silicon (Si) based devices have dominated the electronics industry over the past decades but are not suitable for making lasers due to their optical properties. As an indirect bandgap semiconductor, Si has inefficient optical emission and therefore cannot be used to make a light source on a Si chip. As an alternative, germanium (Ge), incorporated with tin (Sn), can be grown on Si and is currently being used for photonic devices. GeSn exhibits direct bandgap emission at room temperature and is ideal for an on Si light source. However, they suffer from low intensity due to high defect densities which cause nonradiative recombination.

In this work, we study GeSn/Ge/Si samples with varying percentages of Sn. The materials were grown with sub 100 nm thickness resulting in fully strained thin films which reduce the dislocations caused by lattice relaxation. The emission spectrums of these ultra-thin layers were measured using photoluminescence (PL) spectroscopy to probe the quality of the materials as on Si light sources.

3:15pm **TF+CPS+MS+EM-ThA-5 Highly Ordered NiO (111) Films on Sapphire Substrates via Low-Temperature Hollow Cathode Plasma-ALD and Their Post-Deposition Annealing Characteristics**, *Fatih Bayansal, Steven Allaby, Habeeb Mousa, Helena Silva,* ***Necmi Biyikli***, University of Connecticut

Nickel oxide (NiO) is a promising p-type wide band gap semiconductor material for next generation optoelectronic and energy devices. In this study, the growth process and thermal annealing behavior of NiO thin films grown on c-plane sapphire substrates by hollow-cathode plasma-assisted atomic layer deposition (HCP-ALD) method were investigated. $NiCp_2$ was used as the nickel precursor heated at 100°C, and O_2 plasma was preferred as the oxidizing agent under 100W rf-power and 20 sccm flow rate. The films were grown within a substrate temperature range of 100 – 250°C.

The obtained film samples showed high transmittance in the visible spectrum and exhibited strong absorption in the UV spectrum. Optical band gap values determined by Tauc analysis were found between 3.54 and 3.59eV. The refractive indices increased with the growth temperature and reached 2.38, while the extinction coefficient and film porosity decreased for higher temperature films. X-ray diffraction (XRD) analyses revealed that the films exhibit a highly textured structure with exclusive (111) orientation. No peaks belonging to any other phase or crystal plane were observed. Moreover, grazing incidence XRD (GIXRD) measurements showed no detectable peaks, confirming the monocrystalline film character, and suggesting a surface-parallel alignment and potentially dense and thin film morphology. In addition, shifts in the diffraction peaks were observed depending on the growth temperature.

In order to evaluate the thermal stability and performance of the films, the samples grown at 250°C were annealed at 300, 350 and 400°C. Ongoing studies include characterization of electrical properties (Hall effect) such as carrier density, mobility and conduction type as well as crystal structure (XRD, TEM) and chemical composition (XPS). This holistic approach will contribute to understanding the impact of post-deposition annealing on the crystal quality and charge transport properties of NiO films.

This work contributes to the development of optimized p-type oxide semiconductors for transparent electronics and heterojunction-based devices through controlled low-temperature ALD process and post-deposition thermal engineering.

3:30pm **TF+CPS+MS+EM-ThA-6 Textured Growth and Electrical Characterization of Zinc Sulfide on Back-End-of-the-Line (BEOL) Compatible Substrates**, ***Claire Wu***, *Mythili Surendran, Anika Priyoti, Gokul Anilkumar,* University of Southern California*; Chun-Chen Wang,* Taiwan semiconductor Manufacturing Company, Taiwan*; Cheng-Chen Kuo, Cheng-Hsien Wu,* Taiwan Semiconductor Manufacturing Company, Taiwan*; Rehan Kapadia,* University of Southern California*; Xinyu Bao,* Taiwan Semiconductor Manufacturing Company, Taiwan*; Jayakanth Ravichandran,* University of Southern California

Scaling of transistors has enabled continuous improvement in the performance of logic devices, especially with recent advances in materials engineering for transistors. However, there is a need to surpass the horizontal limitations in chip manufacturing and incorporate the vertical or third dimension. To enable monolithic three-dimensional (M3D) integration of high-performance logic, one needs to solve the fundamental challenge of low temperature (<450 °C) synthesis of high mobility n-type and p-type semiconductor thin films that can be utilized for fabrication of back-end-of-line (BEOL) compatible transistors.1 Transition metal oxides are promising n-type materials; however there is a lack of p-type materials that can meet the stringent synthesis conditions of BEOL manufacturing. Zinc sulfide (ZnS), a transparent wide band-gap semiconductor, has shown room temperature p-type conductivity when doped with copper2 and crystallizes below 400oC when grown by pulsed laser deposition (PLD).3 Here, we report growth of crystalline thin films of ZnS by PLD on a variety of amorphous and polycrystalline surfaces such as silicon nitride, (SixNy) thermal silicon dioxide, (SiO2), hafnium dioxide, (HfO2), yttrium oxide (Y2O3), platinum, sapphire (Al2O3), and titanium nitride (TiN). X-ray diffraction shows texturing of ZnS on all surfaces, including when ZnS is directly grown on HF buffered oxide etched silicon. Crystalline quality is investigated using grazing incidence wide angle X-ray scattering measurements. Surface and interface quality is measured using X-ray reflectivity and atomic force microscopy measurements. Electrical characterization of the ZnS films is done by J-V measurements of ZnS on platinum and metal-oxide-semiconductor capacitor (MOSCAP) measurements of ZnS on SiO2 on heavily doped silicon. The J-V measurements indicate low leakage current on the order of 10-8 A/cm-2 with electric field of 0.013 MV/cm2 and the MOSCAP characteristics show bilayer capacitor behavior, which points to ZnS being highly intrinsic with very low unintentional, electrically active point defects. Further work on doping ZnS with copper or other p-type candidate dopants are needed to demonstrate ZnS as a dopable wide band gap semiconductor for channels compatible with BEOL manufacturing. This work showcases the capability of novel thin film growth technique of a wide band-gap sulfide semiconductor in BEOL compatible conditions with potential for technological applications in transistor manufacturing.

1. S. Datta et al., IEEE Micro.39, 6, 8-15 (2019)

2.R. Woods-Robinson et al., Adv. Electron. Mater. 2, 1500396 (2016)

3. M. Surendran et al., Adv. Mater. 36, 2312620 (2024)

3:45pm **TF+CPS+MS+EM-ThA-7 Thermal Atomic Layer Deposition of Molybdenum Phosphide Films**, *John D. Hues, Wesley Jen,* ***Nolan Olaso****, Steven M. Hues, Elton Graugnard,* Boise State University

Aggressive scaling of semiconductor technology nodes has led to copper-based interconnects beginning to approach the maximum scaling limit of the material, beyond which unacceptably high increases in interconnect resistance due to electron scattering at grain boundaries and interfaces begins to cause degradation of device performance. New materials are required for interconnect applications beyond the 7 nm node to produce devices with acceptable signal delay and power consumption parameters. Topological semimetals are one family of materials that are of interest for the replacement of copper in interconnect applications due to the predicted favorable resistance scaling, which results from topologically protected surface states that suppress electron scattering and act as conduction pathways in nanoscale films. This decrease in interconnect resistance has the potential to improve the efficiency of integrated circuits through reduced RC delay and reduced energy consumption, which is under increased scrutiny due to increasing computing demands, such as generative artificial intelligence and cloud computing. In order to aid in the integration of these promising materials into production environments, scalable synthesis methods, such as atomic layer deposition (ALD), are needed. In addition to the development of deposition chemistries for these materials, insight into how processing conditions impact the performance of the resulting film are also of importance. Here, we report on a new thermal ALD deposition chemistry for molybdenum phosphide (MoP) using molybdenum(V) chloride ($MoCl_5$) and tris(dimethylamino)phosphine (TDMAP) at temperatures between 350 °C and 425 °C. In-situ and ex-situ characterization of the resulting films was performed using quartz crystal microbalance (QCM), x-ray photoelectron spectroscopy (XPS), x-ray diffraction (XRD), atomic force microscopy (AFM), scanning electron microscopy (SEM), and four-point probe measurements. QCM measurements demonstrated a linear mass increase of 164 ng/cycle at 375 °C. Film deposition was confirmed through XRD and XPS chemical state analysis. The resulting films were near stoichiometric as determined via XPS. AFM and SEM characterization revealed a polycrystalline morphology with nanoscale grain sizes. Four-point probe measurements of the as-deposited films indicated non-ideal electrical performance which was subsequently improved through post deposition annealing. Although more work is needed to improve electrical performance, this new ALD chemistry may provide a method for the deposition of MoP films at the dimensions required for next generation technology nodes.

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