CHIPS Act : Semiconductor Manufacturing Science and Technologies

Room 207 A W - Session CPS+MS-MoM

Digital Twins and Advanced Packaging for Semiconductor Manufacturing

Moderators: Tina Kaarsberg, U.S. Department of Energy, Advanced Manufacturing Office, **John Lannon**, Micross

9:00am **CPS+MS-MoM-4 An Overview of Advanced Semiconductor Packaging Activities at Arizona State University***, **Christopher Bailey**, Hongbin Yu,* Arizona State University

Arizona State University (ASU) is engaging in all aspects of the chips act including R&D as well as Education and Workforce Development (EWD) activities. At our MacroTechnology Works (MTW) facility, which is a refurbished Motorola Fab, we are installing a 300mm Fan Out Wafer Level Packaging (FOWLP) pilot line based on the DECA M-Series process flow. In addition to this, investments in metrology, EDA, and Multi-Physics modelling have been made to support innovation for future heterogeneous integrated systems.

During this presentation, I will provide an overview of advanced packaging activities underway at ASU which includes projects in the Microelectronics Commons SWAP-Hub program as well as the NAPMP SHIELD-USA project that is pushing the envelop for fan-out wafer level packaging for new substrate technologies with an aim to achieve 0.5um line/spacing and bump pitches as low as 2um. In addition to this, the presentation will detail education and workforce development programs for advanced semiconductor packaging.

9:15am **CPS+MS-MoM-5 Overview of research at the Center for Heterogeneous Integration Research in Packaging (CHIRP) Center***, **Srikanth Rangarajan**,* Binghamton University **INVITED**

The Center for Heterogeneous Integration Research in Packaging (CHIRP) is a leading research center dedicated to advancing the field of heterogeneous integration (HI) for next-generation electronic systems. This talk provides an overview of CHIRP's research activities, focusing on novel packaging technologies, materials, and designs that enable the integration of diverse components with enhanced performance and functionality. We will highlight key projects and recent advancements in areas such as chiplet-based integration, 2.5D/3D packaging, thermal management, and reliability. Furthermore, the presentation will outline CHIRP's collaborative ecosystem and its role in shaping the future of microelectronics through innovative HI solutions.

9:45am **CPS+MS-MoM-7 Re-Shoring Advanced Packaging Capabilities in a Secure Environment***, **John M. Lannon Jr**, Rex Anderson,* Micross Advanced Interconnect Technology

The CHIPS Act has garnered a lot of attention for the re-shoring (or on-shoring) of semiconductor device manufacturing, which includes device manufacturing and downstream packaging, assembly, and test of the devices. Prior to the CHIPS Act, the DoD had been developing its own initiative to de-risk mission critical microelectronics supply chain needs, the Reshore Ecosystem for Secure Heterogeneous Advanced Packaged Electronics (RESHAPE) program. The goal of this program is to ensure the defense industrial base (DIB) has access to a secure, domestic advanced packaging, assembly, and test capability. Initial awards for the program were made late in 2023 for four technical elements: 300mm wafer bumping and 300mm wafer preparation at Micross Advanced Interconnect Technology (a post-CMOS wafer processing facility in North Carolina); Fan-out Wafer-Level Packaging (FOWLP) at the SkyWater facility in Kissimmee, Florida; and Si interposer technology through BRIDG/SkyWater collaboration at the SkyWater facility in Kissimmee, Florida. In this paper, we will provide a brief overview of the RESHAPE program, then focus on the Secure Center for Advanced Packaging Excellence (SCAPEx) project awarded to Micross, covering both current capabilities and future advanced packaging capabilities coming online over the next 12 months.

10:00am **CPS+MS-MoM-8 ML-based Co-design of TSV and TGV Interposers for Advanced Packages***, Pouria Zaghari, Sourish Sinha, **Douglas Hopkins**, Jong Ryu,* North Carolina State University

Copper-filled vias are essential elements in advanced 2.5D and 3D electronic packaging, facilitating reduced form factors and enhanced system performance. This study presents a numerical parametric investigation and a machine learning–driven optimization of through-silicon vias (TSVs) and through-glass vias (TGVs). The optimization targeted three primary performance metrics: copper protrusion, thermal resistance, and electrical parasitics. The coupled influences of aspect ratio (AR) and via pitch were systematically evaluated for both square and hexagonal via array configurations.

The parametric results indicate that glass substrates outperform silicon in mitigating copper protrusion (by up to 47.5%) and reducing mutual capacitance (by up to 67.6%), while TSVs exhibit superior thermal conductivity. A high AR was associated with reduced copper protrusion, whereas low pitch and hexagonal arrays enhanced thermal performance. Conversely, high pitch and low AR configurations were more effective in minimizing electrical parasitics.

For optimization, a conventional genetic algorithm (GA) was benchmarked against a novel online artificial neural network (ANN)–based approach. The ANN method achieved a 61.3% reduction in computational time relative to the GA, underscoring its suitability for high-fidelity optimization of complex electronic packaging designs.

This framework has significant potential for integration into a digital twin environment, wherein a real-time virtual replica of an electronic package can accurately reproduce its electrical, thermal, and mechanical behavior. The computational efficiency of the ANN-based approach enables rapid, high-resolution simulations necessary for real-time digital twin applications—capabilities that are impractical using traditional GA-based optimization due to prohibitive computational demands.

The significance of this work lies in its multidisciplinary co-design methodology, simultaneously accounting for electrical, thermal, and mechanical performance metrics. By leveraging a computationally efficient ANN-based optimization, the framework offers a scalable pathway toward adaptive, self-correcting electronic systems, where digital twins can be employed to predict, monitor, and proactively mitigate potential reliability risks.

10:30am **CPS+MS-MoM-10 Digital Twins and the SRC MAPT2 Chapter on Digital Twins and Applications***, **Robert Baseman**,* IBM Research Division, T.J. Watson Research Center **INVITED**

The semiconductor industry anticipates substantial reductions in manufacturing costs and product times to market as a result of deploying digital twins throughout the design and production ecosystem.Recognizing this, the SMART USA Institute was established as part of the CHIPS Act to accelerate efforts to develop, validate, and use digital twins to improve domestic semiconductor design, manufacturing, advanced packaging, assembly, and test processes.

Here we summarize Chapter 12 of the Semiconductor Research Corporation’s Microelectronics and Advanced Packaging Technologies Roadmap2 (SRC MAPT2), a collaborative effort of experts from academia, industry, and national labs.This new Chapter in MAPT2 is intended to provide a digital twin focus to the industry Roadmap, to inform the SMART USA Institute strategy and to illustrate how digital twins will support the US NSTC Strategic Plan and the National Strategy on Microelectronics Research.

Digital twins of relevance to the semiconductor industry and considered in the Chapter include twins of a vast scope: from twins of atomic scale surface chemistry processes with a characteristic time scale of picoseconds to twins of global supply chains with a characteristic timescale of years.

The Chapter characterizes the state of the art, future industry requirements, challenges to be overcome, and enabling technical directions for twins *per se,* infrastructure enabling development & deployment of twins, and applications of twins.The Chapter includes some perspectives on assessing the impact of twin deployment and concludes with some illustrations of how digital twins will support several domestic strategic initiatives.

11:00am **CPS+MS-MoM-12 Digital Twins Meet Materials Science: Real-Time AI Analysis for Advanced Manufacturing***, **Jeff Terry**,* Illinois Institute of Technology

We have developed an artificial intelligence (AI)-driven methodology for the automated and reliable analysis of advanced materials characterization measurements, including Extended X-ray Absorption Fine Structure (EXAFS), Nanoindentation, X-ray Emission Spectroscopy (XES), and X-ray Photoelectron Spectroscopy (XPS). These techniques are critical for probing

the chemical, structural, and mechanical properties of materials at the nanoscale and are commonly deployed across semiconductor fabrication lines for quality assurance, process control, and failure analysis.

At the heart of our approach is a genetic algorithm capable of extracting physically meaningful structural parameters by fitting experimental spectra to a curated set of candidate chemical configurations. Analysts provide a preliminary list of potential compounds and corresponding computational inputs, after which the algorithm iteratively refines the model to best match the observed data. This process is implemented in our open-source Python analysis framework, **Neo**, which is designed to support modular, high-throughput, and reproducible analysis pipelines.

Importantly, Neo interfaces directly with the **XPS Oasis** and **XES Oasis** databases—comprehensive, structured repositories of curated spectral reference data. These databases allow Neo to draw from a rich library of previously characterized materials and electronic structures, significantly enhancing its ability to identify subtle differences in chemical states and bonding environments. This capability is especially valuable in semiconductor production, where minor variations in composition or surface chemistry can have outsized impacts on device performance and reliability.

By embedding this AI-enabled analysis tool within production environments, manufacturers can achieve **real-time, in-line monitoring** of materials during fabrication. Moreover, by streaming these insights into **digital twin platforms**, facilities can build continuously updated virtual models of the physical production line. These models enable predictive analytics, fault detection, process optimization, and adaptive control—ultimately reducing downtime, improving yield, and enhancing materials traceability throughout the supply chain.

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