Plasma Science and Technology
Room 201 ABCD W - Session PS1-TuA

Plasmas in Advanced Packaging

Moderators: Catherine Labelle, Intel Corporation, **Eric Miller**, IBM

2:15pm **PS1-TuA-1 Critical Plasma Processing Steps for Fusion and Hybrid Bonding Applications*, James Papanu,*** Tokyo Electron Corporate Innovation Division / Tokyo Electron Kyushu, Ltd., Japan*; Scott Lefevre, Jeffrey Shearer,* TEL Technology Center America*; Michiko Nakaya,* Tokyo Electron Corporate Innovation Division, Japan*; Yousuke Mine, Yutaka Yamasaki,* Tokyo Electron Kyushu, Ltd., Japan*; Takayuki Ishii,* Tokyo Electron Kyushu, Ltd, Japan*; Christopher Netzband,* TEL Technology Center America*; Yuji Mimura,* Tokyo Electron Kyushu, Ltd., Japan*; Chikashi Aoyagi,* Tokyo Electron Ltd., Japan*; Ilseok Son, Angelique Raley, Sitaram Arkalgud,* TEL Technology Center America **INVITED**

Die-to-wafer (D2W) and wafer-to-wafer (W2W) hybrid and fusion bonding are integral to advanced packaging applications. Prior to bonding, for both D2W and W2W approaches, surface preparation is performed to facilitate the bonding process. Surface preparation consists of plasma activation and wet cleaning and hydration process steps. These steps are critical to obtain good interface quality and in turn high yield bonding that is void-free with high bond strength. Plasma surface activation is typically a relatively short, low power process. Nonetheless, the plasma source hardware and process conditions must be optimized to provide sufficient activation without roughening the dielectric layer (fusion and hybrid bonding) or sputtering and/or heavily oxidizing the bond pad Cu (hybrid bonding).

D2W bonding is required for chiplet heterogenous integration, and also offers the potential for yield improvement by the use of known good die for high bandwidth memory (HBM) and CMOS image sensor (CIS) applications. For D2W bonding, singulated die are bonded directly onto the target wafers. However, the quality of the die singulation process directly impacts the bonding yield. Defectivity levels for traditional saw dicing are too high for high volume D2W manufacturing. As such, advanced singulation techniques, such as plasma dicing are an essential part of the D2W ecosystem. For plasma dicing, there are two approaches, referred to as dice before grind (DBG) and dice after grind (DAG). For DBG, the etching process is performed before wafer thinning. The etching process trenches or grooves the full thickness wafers, and the dies are then singulated during the backgrind thinning process. For DAG, the etching process directly singulates or dices the thinned wafer, landing on a carrier. Consequently, the DBG and DAG have different process requirements and integration challenges.

In this paper, an overview of the fundamental mechanisms, chamber hardware factors, key process parameters, and process integration considerations for surface activation and plasma dicing steps will be presented. In addition, implementation of surface activation plasma for onto bonding cluster tools will be discussed.

2:45pm **PS1-TuA-3 Plasma processing opportunities in the era of Chiplet and Advanced Packaging for AI application*, Fee Li Lie,*** *Shravana Kumar Katakam, Yann Mignot, Eric Perfecto,* IBM Research Division, Albany, NY **INVITED**

The evolution of artificial intelligence (AI) and machine learning (ML) technologies has exponentially accelerated the computing and memory power needed to train AI systems. This leads to larger and larger System on Chip (SoC) dies, some of which are hitting the lithography reticle limit or experiencing area-driven reduction of die yield. There is an additional need for very high bandwidth between processors and large arrays of memory. One emerging solution is to disaggregate large SoC dies into chiplets and re-connect them using advanced packaging techniques. Interconnection between chiplets can occur directly on the package substrate (“2D”), on an interposer (“2.xD”), through stacking of multiple chiplets (“3D”), or potentially a combination of these different technologies depending on application requirements. Die to die interconnect bandwidth and latency are key and we can broadly categorize these connections as lateral or vertical. Lateral interconnection is usually achieved through dual damascene Cu wiring in hard dielectric or plated-up Cu wiring in organic dielectric. Vertical interconnection is usually achieved by using “through” vias, namely Through Silicon Via (TSV), Through Dielectric Via (TDV), or Through Mold Via (TMV), in conjunction with fine pitch micro bump or Hybrid bonding for die to die joining. In this talk, we will discuss plasma processing opportunities in the era of Chiplet and Advanced Packaging, with emphasis on 3D integration with active Si interposers. We will introduce an overview of plasma processes typically used in 3D integration, and then review scope of needed improvements for some of the critical processes such as TSV RIE, Si thinning, and TSV reveal. Finally, emerging plasma applications for hybrid bonding such as plasma dicing will be introduced.

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