Bias stress instability of InGaZnO thin film transistors for stackable 1capacitor-1transistor dynamic random access memory

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Recently, the demand for high-performance, low-power memory has increased with the growth of artificial intelligence and deep learning technology. The dynamic random access memory (DRAM) industry maintains the scaling trend through cell size shrink technologies to satisfy this demand. However, the two-dimensional scaling of the DRAM below 10 nm design rule is expected to be challenging due to many technical and performance challenges. Thus, it is required to adopt a stacked structure that can overcome these structural limitations. Amorphous InGaZnO (a-IGZO) has emerged as a feasible channel material for stackable DRAM due to its very low off-current and higher electron mobility compared to polycrystalline silicon.

Previous studies have mainly reported the improvement of the electrical characteristics of a-IGZO channel as a single thin film transistor (TFT). However, few reports have been made on a-IGZO TFTs' output current, threshold voltage (V_{th}) variation, and instability related to charging operation when TFT is directly connected to the capacitor.

This study implemented a planar 1T-1C DRAM structure to simulate the write/read operation of the conventional DRAM and investigated the electrical characteristics of a-IGZO TFTs during the DRAM operation process, where the TFTs have bottom-gate staggered structure using the sputtered a-IGZO channel. The TFT adopted a 20 nm-thick bottom gate with different metals and a 10 nm-thick high dielectric constant (k) dielectric film (HfO_2 and Al_2O_3) as the gate insulator. The drain electrode of the transistor was connected to the top electrode of the capacitor, and the gate insulator thin film of the transistor shared the dielectric film of the capacitor. Al_2O_3 was selected as the passivation layer, which also contributed to achieving the controllability of V_{th}[1] and stability of V_{th} under bias stress.

This work investigates whether these improvements of a-IGZO TFTs have comparable impacts under bias stress conditions caused by the charge stored in the capacitor of 1T-1C DRAM application. The findings of this study will contribute to the understanding of a-IGZO as an alternative channel material for the next DRAM transistor.

References

[1] Rha et al. "Variation in the threshold voltage of amorphous-$In_2Ga_2ZnO_7$ thin-film transistors by ultrathin Al_2O_3 passivation layer." Journal of Vacuum Science Technology B, 31, 061205 (2013).

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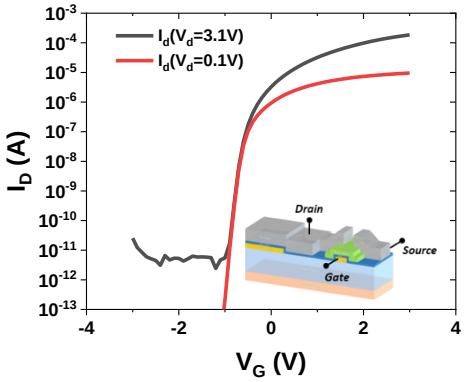

Figure 1. Transfer curve of a staggered bottom gate a-IGZO TFTs: V_D was applied at 0.1 V and 3.1 V with a sweep V_G range of −3–3 V

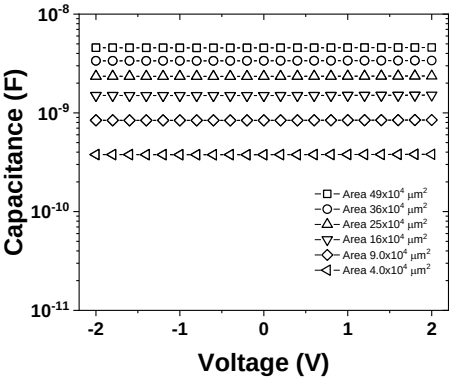

Figure 2. Capacitance-voltage (C-V) curve of MIM capacitor with HfO_2 dielectric. The capacitor area in this measurement is from $4.0x10^4$ μm^2 to $49x10^4$ μm^2