



Figure 1: Scanning electron micrographs of all thermal ALD SiO, TiN, Ru stack (left) and thermal oxide, PVD Ti/W, PVD Cu stack (right) used for Cu electroplating. On the left, the total stack thickness of <math><175\text{ nm}</math> of ALD is not visible on this scale, however the fact that Cu has been electroplated and remains well adhered are evidence of success. The image on the right shows two defects resulting from the PVD Cu barrier/seed stack. The electroplating has narrowing at the top caused by a gradient in the Cu seed layer thickness and voids at the bottom, likely caused by a thin Cu adhesion layer (either Cu or Ti/W) resulting in delamination of the Cu creating a void.