

Fig. 1. Core-shell architecture for UVC LED.

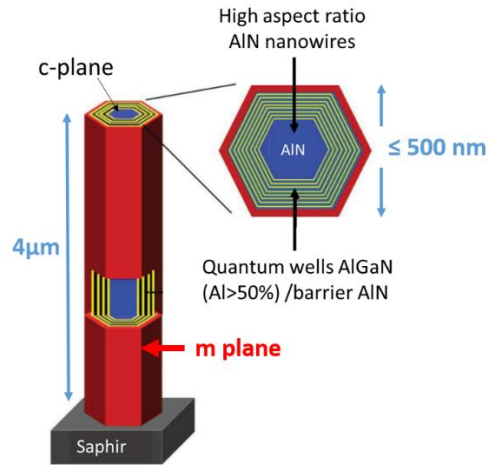


Fig. 2 AIN nanowires profiles obtained with two different carrier wafers. (a) straight profile and no passivation layer using Si CW. (b) tapered profile and passivation layer with Si_3N_4 CW.

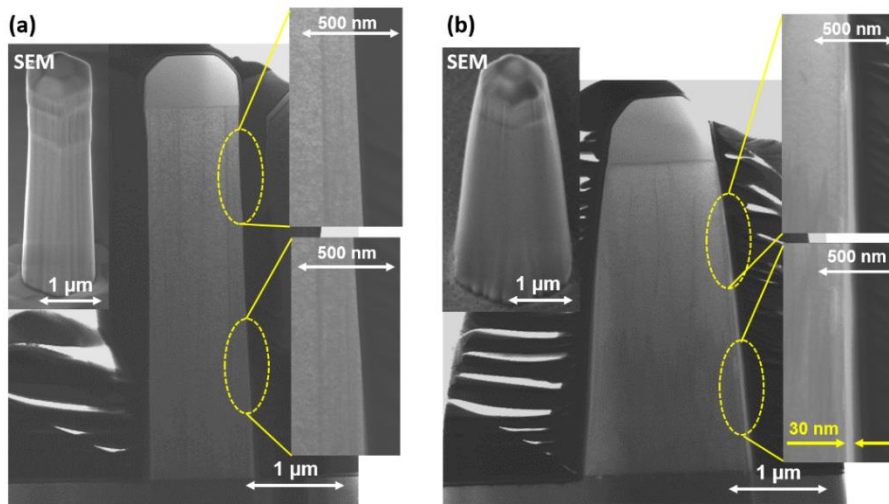


Fig 3. Nanowires profile evolution from tapered to straight or reentrant with source power increasing.

