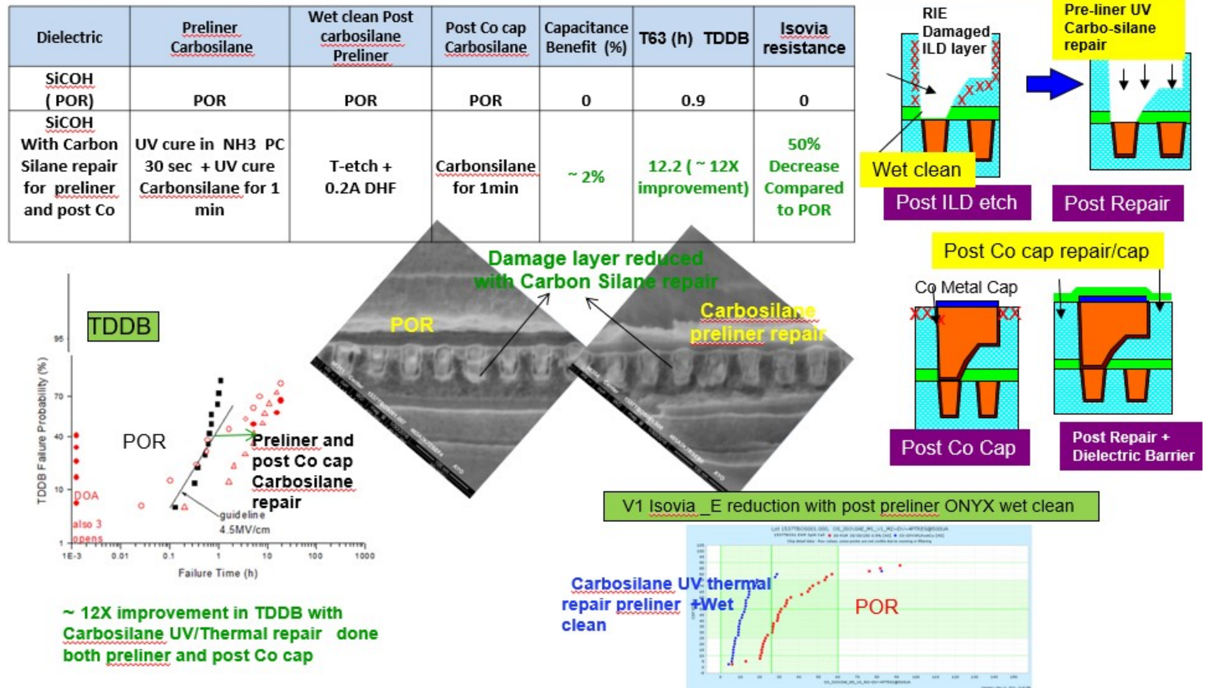
Selective deposition of low k SiCOH and surface sialylations repair of low k dielectrics for nano Cu interconnects. (supplement figures 1-5)



Dielectric	Preliner Carbosilane	Wet clean Post carbosilane Preliner	Post Co cap Carbosilane	Capacitance Benefit (%)	T63 (h) TDDB	Isovia resistance
SiCOH (POR)	POR	POR	POR	0	0.9	0
SiCOH With Carbon Silane repair for preliner and post Co	UV cure in NH3 PC 30 sec + UV cure Carbonsilane for 1 min	T-etch + 0.2A DHF	Carbonsilane for 1min	~ 2%	12.2 (~ 12X improvement)	50% Decrease Compared to POR

Figure 1- Summary of Typical representative processes and improvement in Capacitance and TDDB in 36 nm Pitch devices with UV/Thermal Cure rbonsilane sialylation repair process implement post RIE damage and Selective Co eposition.

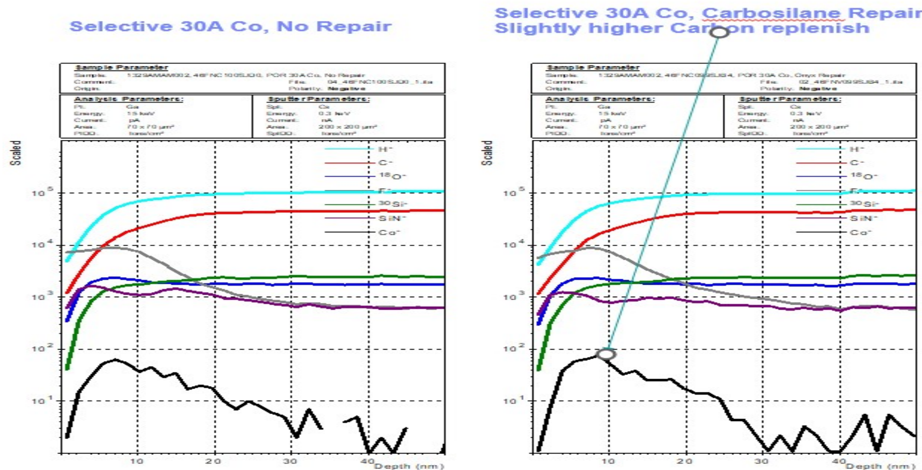


Figure 2- Time of Flight SIMS Analysis of SiCOH surface after Selective Co process showed some increase in carbon concentration on surface post surface Sialylation repair by Carbosilane precursor.

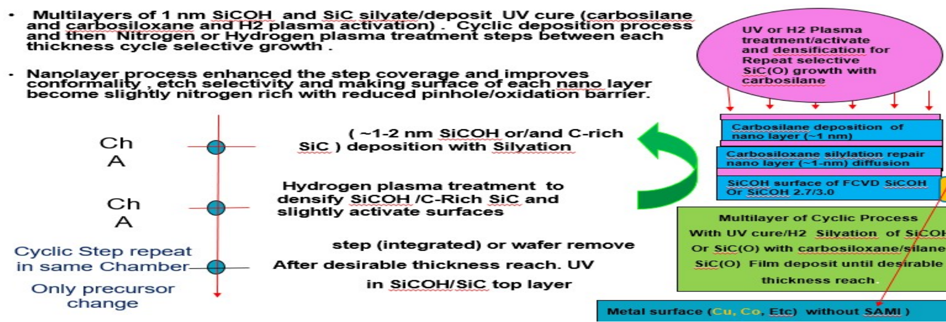


Figure 3- Graphical illustration of Integrated 1x cycle Carbo-siloxane sialylation repair and 10x cycles for ~6nm SiC(O) selective deposition with carbo-silane.

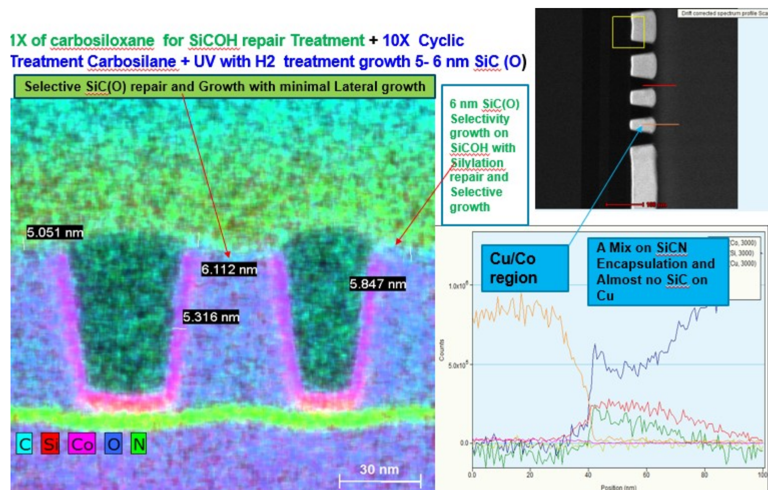


Figure 4- Sialylation and SiC(O) Selective deposition on SiCOH_Co Capped Cu patterned surface result with Scan Transmission electron Microscopy, Electron Emission Loss Spectroscopy Analyses: sialylation repair penetrates into SiCOH and Selective growth of 6 nm SiC(O) after 10x cyclic processing steps.

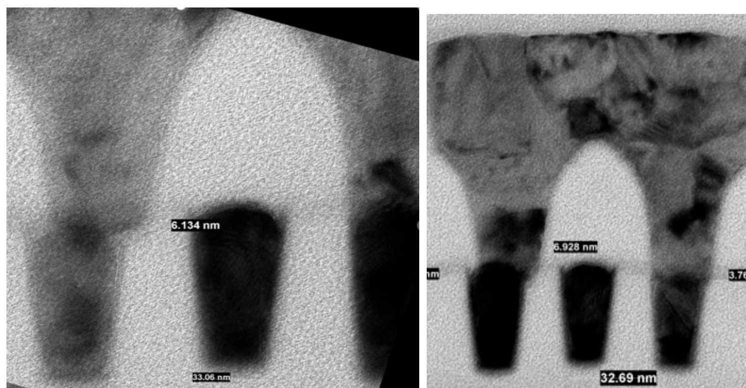


Figure 5- Representative of Fully Aligned Via structure fabricated after Integrated sialylation and Selective deposition of 4 nm SiC(O) with UV/Thermal Assisted Vapor Processing. Even with Slight/minor misalignment, the selective SiC(O) deposition provide >6 nm minimum spacing.