

Supplemental document

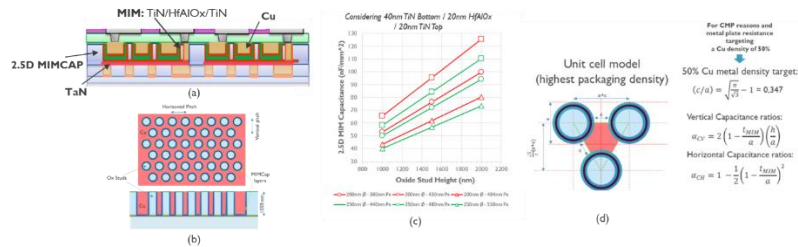


Fig. 1. (a) Illustration of 2.5-D MIMCAPs. (b) Top view (above)/profile (below) of hexagonal grid of oxide studs, the remaining space is filled with Cu. (c) Simulation graph of capacitance density vs oxide stud height (red curve: 200 nm stud CD, square-380nm pitch, circle-430 nm pitch, triangle-484 nm pitch; green curve: 250 nm stud CD, square-440nm pitch, circle-480 nm pitch, triangle-550 nm pitch). (d) Illustration of the relation between capacitance ratio and CD, pitch, oxide stud height.

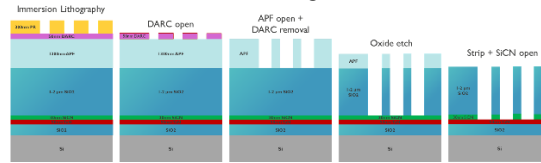


Fig. 2. Schematic of HAR oxide studs etch flow.

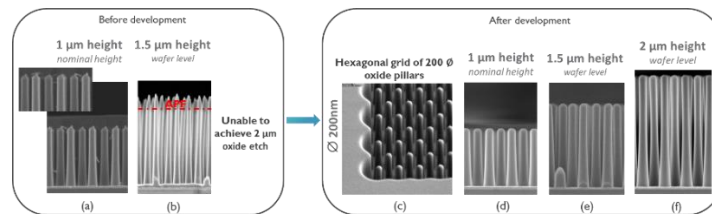


Fig. 3. SEM images illustrating 200nm CD and 380nm pitch studs: (a) the cross section of 1µm height oxide studs with previous etch flow, showing the residuals on the top resulting from the redeposition of TaN on APF; (b) the cross section of 1.5µm height oxide studs with 200nm APF left on the top after oxide etch and before strip with the starting recipe. It shows the APF mask is not enough to form 2µm oxide studs yielding too small CD/excessive slope/bending of the oxide studs. (c) The top view of 1µm height oxide studs after the etch development; (d), (e), (f) show the cross sections of oxide studs with heights of 1.0, 1.5 and 2.0µm respectively, after etch development.

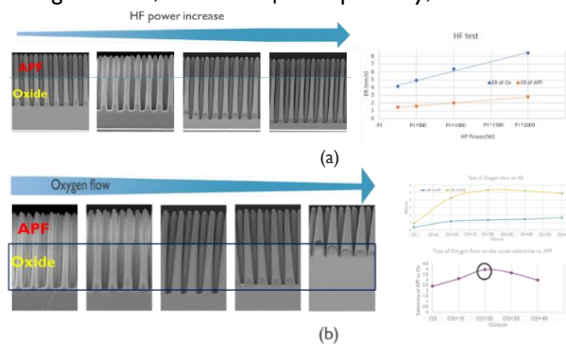


Fig. 4. (a) Experimental results of high frequency (HF) power test on oxide stud open step, the left part shows SEM images, the right part displays the graph of HF power effect on etch rate. (b) Experimental results of the Oxygen gas flow test, the left part shows SEM images, and the right part presents the graph of Oxygen effect on the oxide and APF etch rate (top), and the oxide selectivity to APF (bottom).

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Reference:
 [1] H. Lin, D. Velenis, P. Nolmans, X. Sun, F. Catthoor, R. Lauwereins, G. Plas, E. Beyne. (2022). 84%-Efficiency Fully Integrated Voltage Regulator for Computing Systems Enabled by 2.5-D High-Density MIM Capacitor. IEEE Transactions on Very Large-Scale Integration (VLSI) Systems. 30(5), pp1-5.
 [2] H. Lin, D. Velenis, P. Nolmans, X. Sun, F. Catthoor, R. Lauwereins, G. Plas, E. Beyne. (2021). 91.5%-Efficiency Fully Integrated Voltage Regulator with 86fF/µm²-High-Density 2.5D MIM Capacitor. Conference: Symposia on VLSI Technology.