Electronic Materials and Photonics
Room 114 - Session EM+AP+TF-WeA

CMOS and BEOL - Advances in Materials Integration and Devices

Moderators: Erica Douglas, Sandia National Laboratories, **Cheng Gong**, University of Maryland College Park

2:15pm **EM+AP+TF-WeA-1 All-Acoustic and Single-Chip Radio Frequency Signal Processing via Heterogeneous Integration of Semiconductors and Piezoelectric Materials***, **Matt Eichenfeld,*** University of Arizona **INVITED**

Radio frequency front-end signal processors are the workhorses of modern communications and sensing, providing the signal processing link between data and the radio waves that carry that data between transmitters and receivers. These front-end processors typically use a mix of piezoelectric acoustic microchips and semiconductor transistor microchips to achieve the many different functions they need to encode and decode information. Because of the very disparate materials used, these different chips are assembled at the system level into so-called multi-chip modules, and this system-level integration greatly increases the size of RF systems and degrades their performance. In this talk, I will describe how we have used heterogeneous integration of semiconductor materials with piezoelectric materials such as lithium niobate to create the first-ever comprehensive platform for radio-frequency signal processing with gigahertz frequency acoustic waves. This all-acoustic approach means that the entire front-end processor can be made on a single chip, paving the way towards wireless technologies with more than a 100x reduction in form-factor, as well as increased performance and lower power consumption. It is also a sandbox for studying and engineering the complex interactions between electrons and phonons in solid state materials that may lead to new discoveries and innovations in electronics, phononics, and thermal transport.

2:45pm **EM+AP+TF-WeA-3 Breaking the Quantum Conductance Barrier in CMOS Interconnect Design***, **William Kaden,*** University of Central Florida

Moore's law miniaturization has greatly amplified the importance of interconnect resistance as the limiting factor controlling computational power consumption and clock-speed limitations. The most recent inflection point occurred when cross-sectional wire dimensions miniaturized below the electron mean free path for charge transport within the wire. This has led to deleterious deviations from bulk resistivity scaling trends as uncontrolled surface scattering contributions have become increasingly non-negligible. Searches for suitable replacements to copper for bottom level interconnects have emerged as a direct consequence, with a figure of merit consisting of $\lambda^*\rho_0$ emerging as a primary screening criteria used to find materials best balancing bulk and surface contributions to wire resistivity within this size regime. With decreasing wire cross-sections has also come decreasing grain size, such that grain-boundary scattering also accounts for a significant fraction of the resistivity size effect trends observed in nanowire test-structures. Despite these challenges introduced by miniaturization, further miniaturization of bottom layer interconnect lengths now has the potential to beneficially reduce wire resistance via a fundamental change in charge-transport enabling ballistic conduction to emerge as wire lengths also begin to decrease below electron mean free paths. For reference, bottom layer interconnects are now comparable in length to the room temperature mean free path of bulk copper (~40 nm). Nonetheless, current interconnects do not support quantum conduction due to several non-phononic scattering contributions associated with interactions with grain boundaries, wire surfaces, and defects, such that the effective electron mean free path observed in industrially fabricated nanowires is far less than that of the bulk metals from which they are composed. To successfully leverage the potential for quantum conductance at current interconnect dimensions, non-phononic contributions to resistivity must first be mitigated. Our group has aimed to achieve this through the creation of high-quality single-crystalline nanowire test-structures, for which we have established process-mediated phenomenological control over surface scattering specularity. To achieve this, our group has developed and characterized heteroepitaxial Ru(0001) thin-films deposited on Al_2O_3(0001) wafers, leveraged electron-beam lithography to subtractively pattern nanowire devices, and compared wire resistance observations at varied temperatures to establish ballistic contributions to conductance as a function of wire length and temperature.

3:00pm **EM+AP+TF-WeA-4 "Suboxide MBE" — A Route to p-Type and n-Type Semiconducting Oxides at BEOL Conditions***, **Darrell Schlom,*** Cornell University

In this talk* I will describe a variant of molecular-beam epitaxy (MBE)—"suboxide MBE"—that makes it possible to deposit *p*-type and *n*-type semiconducting oxides with excellent structural perfection epitaxially at back end of line temperatures. In suboxide MBE the molecular beams consist of pre-oxidized elements (suboxides) that help navigate kinetic pathways. For example, supplying a molecular beam of indium suboxide (In_2O) eliminates the rate limiting step of conventional MBE to the growth of In_2O_3—the oxidation of indium to its suboxide—and by skipping this step growth with excellent crystallinity, surface smoothness, and at a low growth temperature are achieved. Similarly, Sn^{2+}-based *p*-type oxides that are challenging to deposit due to this delicate oxidation state may be deposited at BEOL conditions by utilizing suboxide MBE. In addition to extensive structural characterization, electrical characterization and working transistors will also be shown.

*This work was performed in collaboration with coauthors from the groups of: S. Chae, K. Cho, S. Datta, F. Giustino, C. Guguschev, G. Hautier, F.V.E. Hensling, D. Jena, I.M. Kankanamge, Z.K. Liu, D.A. Muller, H. Paik, X.Q. Pan, N.J. Podraza, Y.E. Suyolcu, P.A. van Aken, P. Vogt, M.D. Williams, H.G. Xing, and P.D. Ye

3:15pm **EM+AP+TF-WeA-5 Epitaxial Metastable Cubic CO(001)/MgO(001): Potential Interconnect Conductor***, **Anshuman Thakral,*** *D. Gall,* RPI

The phase composition of Co layers deposited by magnetron sputtering is studied as a function of processing gas (Ar or N_2), temperature T_s = 100-600 °C, and substrate [Al_2O_3(0001), MgO(001) and SiO_2/Si] in order to determine the energetics for thin film synthesis of metastable fcc cobalt which has been theoretically predicted to be the most conductive metal in the limit of narrow interconnect lines. Nitrogen gas facilitates the growth of the metastable cubic phase particularly at T_s > 200 °C. Cubic MgO(001) substrates suppress nucleation of hcp Co grains, resulting in fcc Co even in an Ar atmosphere. The highest crystalline quality epitaxial fcc Co(001) layers are obtained with deposition on MgO(001) in 5.0 mTorr N_2 using T_s = 400 °C during deposition, followed by vacuum annealing at 500 °C. The resistivity size effect in FCC Co is quantified with transport measurements at 295 and 77 K. Data fitting with the Fuchs-Sondheimer model of the measured resistivity ρ vs thickness d = 5 – 1000 nm for single-crystal Co(001)/MgO(001) layers indicates an effective electron mean free path λ_{eff} = 27± 2 nm at 295 K and a room-temperature bulk resistivity ρ_o = 6.4 ± 0.3 μΩ-cm. At 77 K, the reduced electron-phonon scattering yields a smaller ρ_o = 1.3 ± 0.1 μΩ-cm and a larger λ_{eff} = 79 ± 6 nm. The resulting benchmark quantity $\rho_o\lambda_{eff}$ = 17.4×10^{16} and 10.2×10^{16} Ω-m^2 at 293 and 77 K, respectively, is 4-6 times larger than the first-principles predictions. The measured ρ_o for fcc Co is identical to that of the stable hcp Co phase. However due to the high effective mean free path and resulting high $\rho_o\lambda_{eff}$ values, cubic Co does not outperform hcp Co for interconnect applications. The developed method for growth of epitaxial fcc Co(001) layers provides opportunities to study this metastable material for potential spintronic applications.

3:30pm **EM+AP+TF-WeA-6 Characteristics of Reconfigurable FETs Implemented on Bulk Silicon Using Reduced Pressure CVD***, S. Lee, S. Kim, J. Park, W. Lee, **Dongwoo Suh,*** Electronics and Telecommunications Research Institute, Republic of Korea

As semiconductor process technology advances, tremendous efforts have been made in device engineering to mitigate the issue of integration density. One of the representative and prospective solutions is the novel device of reconfigurable FET, single FET working either as n- or p-MOSFET according to the polarity of gate bias. Because reconfigurable FET stands in need of intrinsic source/drain and channel, it has been fabricated on expensive and size-limited SOI wafers. Furthermore, its application is restricted to special devices leaving contemporary CMOS technology irrelevant. In the present study we fabricated reconfigurable FETs on bulk silicon wafers using a lateral epitaxial growth technique unleashing its application potential.

Starting with 6-inch p-type (100) wafers covered with the oxide layer of 0.1 μm, we etched out the oxide layer to form a small seed zone following the epitaxial growth of intrinsic silicon from it using reduced pressure CVD. Having scrutinized the grown epilayer with high resolution transmission electron microscopy, we ensured that its crystal quality was very good in spite of local stacking faults. After planarization of the grown epilayer with CMP, we made Schottky contacts of titanium silicide both on the surface footprint of source and drain to form reconfigurable FET. Our device

consists of single control gate in the center of the channel and two polarity gates placed symmetrically around it.

Current-voltage properties are investigated at the drain voltage of 1 Volt for various polarity gate potential. We obtained clear reconfigurable characteristics of n-MOS under positive gate bias and p-MOS vice versa reaching at the maximum current of 0.1 μA/μm for nMOS and 0.8 μA/μm for p-MOS operation. Transfer characteristics show higher current in p-MOS operation on the contrary to conventional FET. This result is caused by the difference of Schottky barrier height of titanium silicide for n-type (0.61 Volts) and P-type (0.49 Volts). Current levels are small overall because spatial gaps between two adjacent polarity and control gates are inevitably formed during the fabrication process. Notwithstanding the gap issue, our device can reduce the load of device integration. In addition, the present device can be a strong candidate for the mitigation of power issue in IC chips when cutting-edge CMOS technology is applied appropriately.

This work was supported by a National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIT)(Ministry of Science and ICT, NRF-2019M3F3A1A02076911).

4:15pm **EM+AP+TF-WeA-9 Forward Bias Annealing of Proton Radiation Damage in NiO/Ga_2O_3 Rectifiers**, ***Jian-Sian Li,*** *C. Chiang, H. Wan,* University of Florida, Gainesville*; M. Rasel, A. Haque,* Pennsylvania State University*; J. Kim,* Seoul National University, Republic of Korea*; F. Ren,* University of Florida*; L. Chernyak,* University of Central Florida*; S. Pearton,* University of Florida

17 MeV proton irradiation at fluences from 3-7 x10^{13} cm^{-2} of vertical geometry NiO/β-Ga_2O_3 heterojunction rectifiers produced carrier removal rates in the range 120-150 cm^{-1} in the drift region. The forward current density decreased by up to 2 orders of magnitude for the highest fluence, while the reverse leakage current increased by a factor of ~20. Low-temperature annealing methods are of interest for mitigating radiation damage in such devices where thermal annealing is not feasible at the temperatures needed to remove defects. While thermal annealing has previously been shown to produce a limited recovery of the damage under these conditions, athermal annealing by minority carrier injection from NiO into the Ga_2O_3 has not previously been attempted. Forward bias annealing produced an increase in forward current and a partial recovery of the proton-induced damage. Since the minority carrier diffusion length is 150-200 nm in proton irradiated Ga_2O_3, recombination-enhanced annealing of point defects cannot be the mechanism for this recovery, and we suggest that electron wind force annealing occurs.

4:30pm **EM+AP+TF-WeA-10 Studies of the Effects of Doping and Nanolamination on the Temperature Coefficient of Resistivity of Ru-TiO_2 Thin Films**, *S. Berriel,* ***Gouri Syamala Rao Mullapudi,*** University of Central Florida*; N. Rudawski,* University of Florida*; P. Banerjee,* University of Central Florida

High precision electronics require the use of materials with constant resistivity across a wide range of temperatures. The metric of change of resistivity with temperature is known as temperature coefficient of resistivity (TCR). Low TCR is highly desirable for applications such as wearable strain sensors, automobile electronics, and microelectronics. Materials of low TCR can be difficult to come by. However, metals exhibit positive TCR, and semiconductors and insulators exhibit negative TCR. Thus, a combination of metallic and semiconducting materials could be used to create a net low TCR.

Atomic layer deposition (ALD) is a method well-suited to the task of tuning thin film composition between metal and insulator. To this end, we have studied the effect of nanolaminate-structured vs doped films on TCR for a temperature range spanning from 80 K to 420 K. The compositions of the thin films have been finely controlled by combining Ru - a metal, and TiO_x - an insulator, using a Veeco Fiji G2 ALD chamber. Two types of films were made: First, a series of nanolaminates of 30 nm total thickness were synthesized with 50/50 composition Ru/TiO_x while varying thickness of individual layers. Second, a set of films were made by dosing small amounts of TiO_x into a predominantly Ru film totaling 30 nm thickness. The thickness of the total film and individual layers were monitored using *in situ* spectroscopic ellipsometry. The films have been further investigated via temperature-dependent van der Pauw, XRD, and TEM measurements to determine a cross-over from metallic to insulating behavior thus, precisely targeting a composition that produces low TCR behavior.

4:45pm **EM+AP+TF-WeA-11 Dorothy M. and Earl S. Hoffman Scholarship Awardee Talk: Determination of Band Offsets at the Interfaces of NiO, SiO_2, Al_2O_3 and ITO with AlN**, ***Hsiao-Hsuan Wan***[1], *J. Li, C. Chiang, X. Xia, D. Hays,* University of Florida*; N. Al-Mamun, A. Haque,* Pennsylvania State University*; F. Ren, S. Pearton,* University of Florida

The valence and conduction band offsets at the interfaces between NiO/AlN, SiO_2/AlN, Al_2O_3/AlN and ITO/AlN heterointerfaces were determined via x-ray photoelectron spectroscopy using the standard Kraut technique. These represent systems which potentially would be used for p-n junctions, gate dielectrics and improved Ohmic contacts to AlN, respectively. The band alignments at NiO/AlN interfaces are nested, type I heterojunctions with conduction band offset of -0.38 eV and valence band offset of -1.89 eV. The SiO_2 /AlN interfaces are also nested gap, type I alignment with conduction and offset of 1.50 eV and valence band offset of 0.63 eV. The Al_2O_3/AlN interfaces are type-II (staggered) heterojunctions with conduction band offset -0.47 eV and valence band offset 0.6 eV. Finally, the ITO/AlN interfaces are type-II (staggered) heterojunctions with conduction band offsets of -2.73 eV and valence band offsets of 0.06 eV. The use of a thin layer of ITO between a metal and the AlN is a potential approach for reducing contact resistance on power electronic devices, while SiO_2 is an attractive candidate for surface passivation or gate dielectric formation on AlN. Given the band alignment of the Al_2O_3, it would only be useful as a passivation layer. Similarly, the use of NiO as a p-type layer to AlN does not have a favorable band alignment for efficient injection of holes into the AlN.

5:00pm **EM+AP+TF-WeA-12 Ferroelectric Al0.2Sc0.8N Diodes on NbN Electrodes Deposited on Sapphire Substrates**, ***Giovanni Esteves,*** *T. Tharpe, T. Young, D. Henry,* Sandia National Laboratories

The emergence of wurtzite ferroelectrics and their scaling below 50 nm has significantly broadened their applications in microelectronics, extending their utility into harsh environments. Ferroelectric aluminum scandium nitride ($Al_{1-x}Sc_xN$) exhibits a unique diode behavior due to its internal switchable polarization. Although AlScN is often accompanied by high coercive fields (E_c) exceeding 3 MV/cm, in contrast to its fluorite ferroelectric counterparts which have E_c values below 1 MV/cm, this high E_c is advantageous for high-temperature microelectronic applications where E_c decreases with temperature. When scaling the thickness below 50 nm, challenges related to achieving high crystallographic texture and accurate device measurements become significant. To address these challenges, this study explores the use of NbN films deposited on sapphire substrates to template the AlScN. X-ray diffraction results reveal that a 24 nm AlScN film inherits its in-plane texture from the underlying NbN film deposited on sapphire. Ferroelectric capacitors were fabricated using 100 nm NbN films as both top and bottom electrodes, and current-voltage (IV) measurements were conducted across multiple capacitors. The ratio of the high resistance state (HRS) to the low resistance state (LRS) was studied as a function of drive voltage, demonstrating changes ranging from 2x to 500x, with some capacitors exhibiting changes well above 1000x. The response between the HRS and LRS is controlled via the partial switching of domains—regions of uniform polarization—within the AlScN film. The promising results of this study pave the way for future applications of AlScN in non-volatile memory devices capable of operating at high temperatures, as well as in analog computing systems. Additionally, continued research into the effects of extreme environments on the ferroelectric response of AlScN will further enhance its potential for robust and reliable performance in demanding conditions. These advancements could significantly impact the development of next-generation microelectronic devices, offering improved functionality.

5:15pm **EM+AP+TF-WeA-13 Optimizing Sputtering Parameters for Tantalum Oxide-Based Resistive Memory: A Design of Experiments Approach**, ***Alireza Moazzeni,*** Wayne State University*; S. Karakaya, A. Khan, G. Tutuncuoglu,* Wayne state university

AbstractThis study optimizes sputtering parameters for Tantalum Oxide-based Resistive Random-Access Memory (TaO_x RRAM, 1<x<2.5) using the Design of Experiments (DOE). By varying oxygen partial pressure (20% and 35%) and DC power (75 W and 250 W), we aim to control device performance metrics like forming voltage and power consumption. Response Surface Methodology (RSM) and Central Composite Design (CCD) were used, with 12 experimental settings and four center points, to explore parameter interactions. The goal is to improve the uniformity and reliability of TaO_x RRAM fabrication for future high-performance memory systems.

[1] **AVS National Student Awardee**

IntroductionTantalum Oxide-based RRAM is a promising non-volatile memory technology for neuromorphic computing, integrating memory and processing to reduce data transfer bottlenecks [1]. TaO_x RRAM's endurance, thermal stability, and scalability make it suitable for various applications [2]. The material's properties can be tuned via thin-film synthesis, particularly by adjusting DC sputtering parameters, allowing control over oxygen vacancies [3, 4]. TaO_x RRAM has achieved fast switching, low power consumption, and high endurance, positioning it as a key technology for future computing systems [5].Despite these advantages, variability, particularly forming voltage, remains a challenge [6]. This is influenced by oxygen vacancy concentration, film thickness, and sputtering conditions [7, 8]. Controlling these factors can reduce device variability [9]. While previous studies looked at oxygen pressure and power independently, this study explores their combined effects on performance.Design of Experiments (DOE), specifically RSM and CCD, was used to optimize the sputtering process within limited operational ranges. CCD allowed efficient exploration of factor values, while RSM provided a framework for modeling multiple variables. The objective is to optimize sputtering parameters, develop a predictive model, and enhance performance metrics like forming voltage and power consumption. Oxygen pressure levels (20% and 35%) and power levels (75 W and 250 W) were chosen with significant separation to identify key trends. Interactions between parameters were also examined, with four center points included for validation, resulting in 12 experimental settings. Figure 1 and Table 1 illustrate the setup and design points.

By optimizing sputtering parameters and investigating their interactions, this study aims to reduce variability in TaO_x RRAM devices and improve performance metrics, contributing to the scalable integration of this technology in next-generation computing systems.

Author Index

Bold page numbers indicate presenter