Plasma Science and Technology
Room 124 - Session PS1-MoM
Plasma Processes for Advanced Logic
Moderators: John Arnold, IBM Research Division, Albany, NY, **Angelique Raley**, TEL Technology Center America

8:15am **PS1-MoM-1 Mechanism of Formation of Roughness During Ru Direct Etching**, ***Miyako Matsui,*** Hitachi Ltd., Japan*; M. Miura, K. Kuwahara,* Hitachi High-Tech Corp., Japan

Scaling of logic devices is still mainly driven by fabricating three-dimensional structures. As device scaling continues, alternative metal interconnects are required to replace Cu that enable reduction of metal pitch at the back end of the line. Ru is a candidate for an alternative interconnect material with metal pitch of 20 nm and beyond because a Ru interconnect is expected to have lower effective resistance than that of a Cu interconnect at such small pitches. Ru is expected to be etched directly, which leads to new scaling boosters such as semi-damascene patterning. In addition, to reduce interconnect resistance, roughness or other damage should be suppressed. In our previous study, we investigated the mechanism of Ru etching and the effects of protection layers formed on the sidewall of a line-and-space Ru pattern etched using Cl_2/O_2-based plasma. In this study, we investigated the mechanism of formation of line-width-roughness (LWR) of a Ru pattern with 32-nm pitch by using Cl_2/O_2-based plasma. We also investigated the influence of mask-pattern roughness and Ru line grain-boundaries on LWR.

We investigated the influence of the roughness of the Si_3N_4 mask pattern on that of the Ru pattern. Before and after Ru etching, LWR was measured by a high voltage CD-SEM, namely, critical-dimension-scanning electron microscope using an incident electron beam at energy of 45 keV. The high voltage CD-SEM was used to simultaneously measure both LWR of the mask-pattern and that of the Ru line. LWR of the mask pattern was measured from the image formed by the secondary electrons and that of the Ru line was measured from the image formed by the backscattering electrons (BSE). These measurements showed that after the Ru etching, LWR of the Si_3N_4 mask pattern and that of the Ru line depend on ion flux, which was adjusted by changing the duty cycle of wafer bias power. When wafer bias power was applied continuously, width of the Si_3N_4 mask became larger and LWR became smaller because the Si_3N_4 mask was widened by the re-deposition of the Si containing by-product. On the contrary, LWR of the Ru line remained mostly constant even when the ion flux was reduced. According to these results, it is necessary to measure LWR of the Ru line from BSE images because LWR of the mask after etching and that of the Ru line are not necessarily correlated.

We also investigated the effect of the grain boundary of Ru on LWR formed at the edge of the Ru line pattern. It was found that sidewall etching tends to proceed from the grain boundary. Accordingly, it is important to prevent the grain boundary from being etched by forming uniform passivation layers on the sidewall.

8:30am **PS1-MoM-2 Enabling Advanced Beol Interconnect Scaling Through Ruthenium Subtractive Etch Patterning**, ***Shravana kumar Katakam,*** IBM Research Division, Albany, NY*; N. Joy, D. Yan,* TEL Technology Center, America, LLC, Albany, NY*; C. Penny, C. Park, K. Motoyama, H. Shobha, Y. Mignot, J. Lee,* IBM Research Division, Albany, NY

With the ever-increasing demand to shrink the critical dimensions (CDs) for advanced technology complementary metal–oxide–semiconductor (CMOS) nodes, the demand to shrink the backend-of-the-line (BEOL) metal line pitch is also increasing. Traditionally the copper (Cu) damascene process has been the main candidate, but modeling results indicate that it may be difficult to scale Cu damascene processes beyond 20nm pitch due to increase in-line resistance. In this regard, ruthenium (Ru) metal is a potential candidate for replacing copper for tighter pitch nodes beyond 20nm pitch. This is attributed to its superior electrical performance compared to traditional copper resistance at these line widths. Ru patterning is through subtractive etch as opposed to damascene process for Cu metals and it has been established that Ru can be patterned easily using chlorine (Cl_2) and oxygen gas (O_2) chemistries due to formation of volatile by products for relaxed pitches, but we run into difficulties as the pitch becomes tighter than 20nm pitch (P20).

The unique challenges during patterning at P20 or less are attributed to significant hardmask swelling from HM re-deposition during the etching process resulting in incomplete Ru etch at the regions affected by HM swelling. Additionally, the oxide re-deposition also results in severe RIE lag demanding a significant amount of over etch compromising pattern fidelity at min pitch structures.

In this work, we have systematically analyzed the changes to the plasma as the etch progresses and identified a possible mechanism for the HM swelling. With the understanding of these mechanisms, we were able to tune the plasma parameters to successfully reduce the HM swelling significantly to the levels that can be tolerated at the tighter pitches of P18 and beyond. We will also enlist some possible approaches to reduce swelling in the context of scaling the Ru etch for even tighter pitches of P16 and beyond.

8:45am **PS1-MoM-3 Atomic Level Control of Plasma Etching Using Various Pulsing and Cyclic Technologies for Leading-edge LSI**, ***Masaru Izawa,*** Hitachi High-Tech Corp., Japan **INVITED**

The cell size of logic LSI has been reduced by adopting Design-Technology Co-Optimization (DTCO) and pitch scaling using double patterning or EUV lithography. Recently, Gate-All-Around (GAA) FETs are being developed for the production of advanced nodes. For the fabrication of leading-edge devices, not only high selective vertical etching but also lateral etching is required. In terms of vertical etching, various pulsing technologies have been investigated, including gas switching using microwave ECR (M-ECR) plasma. For lateral etching, DCR (dry chemical removal) with IR lamp has been applied. This paper discusses some etching challenges in leading-edge devices, particularly related to EUV, DTCO, and GAA.

In EUV tri-layer etching, a mask reconstruction process (MRP) has been developed [1], where area-selective deposition is applied to reduce line-width roughness (LWR) and protect the EUV resist. In Si/SiGe fin etching, an atomic layer etching (ALE) function that includes source, wafer RF bias, and gas pulsing is adopted to achieve a vertical profile with high selectivity. Additionally, hydrogen gas is added to suppress etch depth and CD differences between Si and SiGe fin profiles [2]. In WFM (work function metal) patterning, DC pulse technology is applied to minimize fin damage [3]. The erosion of the fin top is reduced by 57% using this technique, and charging effects are also mitigated by using DC pulses. Furthermore, lateral etching processes using the DCR tool have been studied [4]. For example, etching a 2.5 nm space in Si_3N_4 film using a thermal cyclic ALE scheme was achieved without microloading. Lateral etching of SiO_2 and W has also been investigated.

[1] A. Amend, PS+TF-MoM-10 in AVS 69 (2023).

[2] Y. Ishii *et al*., Jpn. J. Appl. Phys. **57**, 06JC04 (2018).

[3] R. Ochiai *et al*, JSAP spring meeting, 2021, 19a-P04-9.

[4] K. Shinoda *et al*., J. Phys. D **50**, 194001 (2017).

9:15am **PS1-MoM-5 Investigating Plasma Interaction with Ultrathin Polymethylmethacrylate Films for EUV Lithography**, ***Shikhar Arvind****, E. Witting Larsen, P. Bezard, J. Petersen, S. De Gendt,* IMEC, Belgium

State-of-the-art extreme ultraviolet (EUV) lithographic scanners can now pattern with 12 nm half pitch resolution. To enable this high-resolution patterning requires the use of ultrathin (sub-50 nm) photoresists (or resists). This is due to pattern stability concerns of high aspect ratio structures, as well as the exceptionally short depth of focus of high numerical aperture (NA) scanners[1]. But the use of ultrathin resists further complicates pattern transfer as unintended plasma-induced effects during dry etching are more pronounced. The vacuum ultraviolet (VUV) photons generated in plasma are of particular interest for us as they can cause considerable resist modification. A better understanding of the interaction of plasma species, particularly of VUV photons with ultrathin resists is critical for enabling pattern transfer of sub-10 nm features.

Here, we study the impact of VUV photons, argon ions, and argon plasma on a 40 nm thick polymethylmethacrylate (PMMA) film[2]. Using a deuterium lamp, an industrial ion beam etch tool, and an industrial inductively coupled plasma etch tool, we exposed the polymer to VUV photons, ions, and plasma, respectively. The exposed samples were then analyzed for chemical and physical changes using multiple characterization techniques. We observe that the thin resist thickness caused the vacuum ultraviolet photons interact with the entire bulk of the PMMA film, while the ions only affect the surface and near surface region. The photon exposed samples formed smaller polymer fragments at low exposure doses and further started to crosslink at high doses. In contrast, the ion modification led to carbonization of only the top few nanometers of the polymer film, leaving the bottom bulk intact. The plasma exposed sample showed changes characteristic to both vacuum ultraviolet photons and ions, and their synergism. It was stratified with a 1.34 ± 0 .03 nm thick ion-caused

carbonized layer on top of 13.25 ± 0.12 nm photon-induced crosslinked layer. By studying the impact of the individual plasma constituents on ultrathin PMMA, we thus establish a baseline testing methodology for plasma-resist interactions on a simple model system, which we will further deploy on novel resists for EUV lithography.

References:

1. A. Burov, A. Vaglio Pret, and R. Gronheid, "Depth of focus in high-NA EUV lithography: a simulation study," in SPIE Photomask Technology 2022.
2. Shikhar Arvind, Esben W. Larsen, Philippe Bezard, John Petersen, Stefan De Gendt; Impact of vacuum ultraviolet photons on ultrathin polymethylmethacrylate during plasma etching. *J. Vac. Sci. Technol. A* 1 May 2024; 42 (3): 033009. https://doi.org/10.1116/6.0003541

9:30am **PS1-MoM-6 In situ Hard Mask Growth for Break Healing in Ultra-Thin Layers Patterning***, **Rémi Vallat**, P. Bézard, B. Chowrira,* IMEC, Belgium*; A. Fathzadeh,* ku Leuven and Imec, Belgium*; K. Filippidou, L. Souriau, K. Ronse,* IMEC, Belgium

One of the challenges introduced by High NA EUV lithography include defectivity management, particularly when working with (ultra-)thin resists and low EUV exposure doses[1]. Reducing the bridges and breaks density is thus a major point of focus when patterning Line/Space[2]. Traditionally, a descum step is used to remove bridges, resulting in a reduced resist budget for underlayer patterning and leading to the creation of breaks. Therefore, recovering breaks is a strategic capability for defect reduction.

The method consists of patterning an underlayer of suitable thickness for thin resists and run an in situ PECVD process onto this underlayer, selectively to the material below in order to prevent and recover breaks[3]. This way, the hard-mask budget is increased in-situ during the etch process to prevent the formation of breaks while patterning from a thin underlayer (~10nm). This approach is presented in Fig1. Moreover, this method offers a reduced environmental footprint compared to conventional one as thinner ULs need fewer Global Warming Potential gases (GWP)[4]. Patterning of such ultra-thin layers (≤5nm) may come with high bridge/ break density which can be addressed by using this break healing strategy, thanks to in-situ selective HM growth.

In this work, the selectivity of deposition has been achieved, along with a notable decrease in break density and these results are shown in Fig2 and Fig3. However, the presence of additional deposited material brings new challenges. The focus of this work is to investigate the etch mechanisms which occur at the amorphous Carbon layer level, as well as to ensure the pattern transfer uniformity. Preliminary defectivity measurements will also be explored. Applications for both resist types, CAR and MoR, will be discussed. MoR is expected to induce more breaks, particularly problematic for low dose strategies. In addressing this issue, our break healing strategy emerges as a potential candidate for further exploration.

[1] L. Meliet al,*Proc. SPIE*11609, 116090P (2021)

[2] P. De Bisschop, *J. Micro/Nanolithogr. MEMS MOEMS*16, 041013 (2017)

[3] R. Vallat et al, *AVS69*, (PS+NS+FrM-3) (2023)

[4] P. Bézard et al. *Advanced Etch Technology and Process Integration for Nanopatterning XIII*. SPIE (2024)

9:45am **PS1-MoM-7 Plasma Etching of Low K Materials from Room Temperature to -40ºC in Different Fluorine-Based Chemistries***, **Daniel Santos**, C. Vallee,* University at Albany-SUNY

Plasma etching of ultra-low-k materials at aggressive back end of line (BEOL) nodes has become increasingly challenging as plasma induced damage becomes a significant challenge to overcome. Conventional reactive ion etching (RIE) processes usually occur at a temperature near room temperature or higher in which diffusion of radicals will damage low-k materials surface. Alternatively, to limit diffusion mechanisms and prevent damage, cryogenic cooling of a substrate sub <-100 C can be used. However, cooling substrates and controlling surface exposed to plasma to temperature down to -110C in 300 mm etching chamber is a technical challenge. This is why alternative solutions can be found using a low temperature process (down to -60ºC) that behaves like a cryogenic process. For this work we propose to study the plasma etching of low k materials exposed to different fluorine precursors with a substrate temperature going from room temperature to -40ºC. For this purpose, we use a 300 mm dual frequency CCP chamber equipped with a low-temperature electrostatic chuck to conduct our experiments. A shadowing methodology is used to study the plasma/surface reactions with surfaces exposed to radicals only and surfaces exposed simultaneously to radicals and ions. By way of comparison, we chose to use two precursors with very different properties:

1. a fluorocarbon precursor with a high triple point temperature favoring condensation mechanisms, for which we observed a switch from an etching regime to a deposition regime in RIE mode at T = -20ºC. However, the shadowing mask study shows that when the surface is only exposed to radicals, the regime is always the same, deposition.
2. NF_3 gas which has a very low triple point temperature that should not do any deposition. When lowering the temperature, not only is the etching regime not suppressed, but its speed is also increased. This result is explained by the increases of surface coverage by F etching radicals. Using the shadowing methodology, we observed that the etching is highly suppressed at -40ºC compared to room temperature in the absence of ions

Patterned damascene structure are also tested to observe the benefits of low temperature etching. Furthermore, we propose to add hydrogen to NF_3 plasma to promote HF formation and study its impact on low k etching when going from room temperature to -40ºC.

10:00am **PS1-MoM-8 Mitigating Plasma-Induced Damage in Low-K SiCOH Thin Films by Cryogenic Etching Process***, R. Chowdhury, T. Poché, **Seonhee Jang**, Y. Tesfamariam,* University of Louisiana at Lafayette

The integration of semiconductor chips to enhance their performance has led to the widespread use of low-dielectric-constant materials with a relative dielectric constant of k ≤ 3.5, particularly as intermetal dielectric (IMD) materials within multilevel interconnects. This choice aims to minimize resistance-capacitance delays associated with microchip operation. Plasma etching of low-k materials presents a significant challenge due to plasma-induced damage (PID), which can increase the k-value and degrade its quality. This degradation is attributed to factors such as the formation of polar bonds, losing surface hydrophobicity, and carbon depletion.

To mitigate PID damage, this research focuses on reducing the degradation of low-k films during etching by employing a cryogenic process. Cryogenic conditions offer a promising strategy to alleviate PID damage, as etching by-products condense within the pores of the materials, protecting them from plasma-active radicals. By incorporating cryogenic etching process, significant reductions in dielectric degradation can be achieved.

Low-k SiCOH thin films were fabricated using plasma-enhanced chemical vapor deposition (PECVD) of the tetrakis(trimethylsilyloxy)silane precursor at room temperature. Dry etching process was conducted using CF_4, SF_6, CHF_3, and C_4F_8 gases at both room temperature and cryogenic temperatures (up to -120 ℃) in an inductively coupled plasma-reactive ion etching (ICP-RIE) system. Tetraethyl orthosilicate (TEOS) oxide was used as a reference material for calculating etch rates and etch selectivity. The etch selectivity of the SiCOH film over the TEOS was compared between regular and cryogenic etching processes.

Fourier transform infrared (FTIR) spectroscopy identified four prominent bonds in the films which were $C–H_x$ stretching, $Si–CH_3$ bending, Si–O–Si stretching, and $Si–(CH_3)_x$ bending vibration modes. The equivalent damage layer (EDL) was calculated based on the variation in the peak area of $Si–CH_3$ bending and Si–O–Si stretching peaks, with SF_6 gas causing the highest amount of EDL compared to other gases. However, all gases showed a decreasing trend in EDL value when etching was performed at cryogenic temperatures, indicating reduced PID damage.

Electrical properties such as the k-value, leakage current density, breakdown field, and time-dependent dielectric breakdown (TDDB) were also measured to evaluate an improvement in their electrical performance under cryogenic etching confirming reduced PID damage. These findings highlight the potential of cryogenic etching as a promising approach to mitigate PID damage and improve the quality of low-k films.

10:30am **PS1-MoM-10 Investigation of Cryogenic Fluorine-Based Etching of TaN with Selectivity to SiOCH Low-κ***, **Ivo Otto IV**, C. Vallée,* University at Albany College of Nanotechnology, Science, and Engineering (CNSE)

The industry shift from silicon dioxide and aluminum as the respective dielectric and conductor within the back-end-of-the-line (BEOL) interconnect superstructure to SiOCH low-κ dielectric (ULK) and copper improved key metrics such as RC delay, but had inherent integration challenges, one of which was copper diffusion into the ULK film. The solution was the use of diffusion barriers, which are required in current

integration schemes to prevent copper diffusion. TaN is a key diffusion barrier candidate because of strong dielectric adhesion and low in-plane resistivity properties at 2-3 nm thicknesses. Creation of the BEOL interconnect superstructure is completed in cycles to create each metal level, requiring the repeated selective removal of not only copper, but the TaN diffusion barrier, selective to the ULK.

ULK films attain dielectric constant values of between 2-3 by incorporating non-polar bonds ($Si-CH_3$) and pores into their structure, making ULK sensitive to abrasive processes like CMP and physical, ion-assisted etching. Radical-dominated, fluorine etching of TaN with respect to ULK also comes with challenges because of the high volatility of SiF_2, SiF_4, and CF_x ULK etch byproducts. We have previously explored methods to accomplish radical fluorine etching of TaN with selectivity to ULK as an alternative landing process on the ULK, for BEOL integration. Selective deposition of an SiOF film on the ULK film compared to the TaN, while etching the TaN, allowed the selective etching of TaN with respect to ULK. In this work, we explore the use of radical NF_3/SiF_4 discharges, without O_2 addition (1), at sub-zero sample temperatures ranging from -45 °C to 0 °C (2). In this investigation, we seek to reduce the possibility of ULK damage by (1) removal of radical and atomic O interaction with the ULK film and (2) reduce the diffusion path for F to limit F diffusion through any SiF_x deposition on the ULK, and to limit F diffusion within the SiOCH structure itself. *Ex-situ* spectroscopic ellipsometry is utilized to characterize film thickness changes after processing in addition to characterization of changes in film refractive index. *Ex-situ* X-ray photoelectron spectroscopy is used to probe the sample surface to characterize surface film properties, while *ex-situ* Fourier-transform infrared spectroscopy is used to analyze bulk changes in the SiOCH ULK bonding structure. Though this multi-modal investigation, we gain insight in the mitigation of SiOCH ULK damage using an O_2-free, sub-zero process to selectively remove TaN.

10:45am **PS1-MoM-11 Overview of Mutually Compatible Approaches for Sustainable Patterning Process Development**, ***Philippe BEZARD,*** IMEC Belgium*; A. Fathzadeh,* KU Leuven and Imec, Belgium*; R. Vallat, K. Filippidou, E. Gallagher,* IMEC Belgium*; S. De Gendt,* KU Leuven and Imec, Belgium*; F. Holsteyns,* IMEC Belgium

Various approaches can be employed to ensure the sustainability of a process. One option is to utilize new molecules as reactants, aiming to reduce the quantities and/or the impact of emitted fragments in the atmosphere. If suitable candidate molecules are not available, materials that require environmentally harmful gases could be replaced with others that do not rely on such chemistries, for example, replacing a sacrificial SiO2 hard-mask with amorphous carbon. Alternatively, the process flow can be adjusted to avoid the need for these materials altogether.

When changing materials is not feasible, there are several ways to further minimize gas consumption. One approach is to increase throughput without increasing gas flows, often achieved by using higher RF powers or pressures. Thinning down the layer is another option, but this increases the selectivity requirements of patterning steps. In such cases, in-situ reconstruction of the hard-mask, as demonstrated by Vallat et al., can provide thicker, usable hard-masks at the expense of patterning a much thinner problematic layer [1].

To regulate the selectivity of hard-mask deposition and subsequent patterning steps, Transient Assisted Plasma Processing (TAPP) [2] can be employed to significantly reduce gas consumption while maintaining excellent patterning performance and compatibility with High-Volume Manufacturing throughput. Combining these hard-masks with etch processes based on TAPP is particularly appealing because it offers better control over the precursor's fragmentation, resulting in improved deposition selectivity at low substrate temperatures.

In a transient-assisted plasma etching process, these hard-masks can serve as a passivation source by carefully managing their sputtering while allowing the etch to proceed, eliminating the need for often problematic passivating gases. Furthermore, to further eliminate the requirement for environmentally harmful passivation gases, low-density plasmas can be utilized in conjunction with low partial pressure of reactants and overall gas flows. The scarcity of neutral species in such plasmas reduces the risks of bowing and undercutting, requiring minimal passivation to achieve the necessary patterning performance.

This paper will present an overview of the characteristics of these various approaches and illustrate how they can be combined to significantly reduce the consumption of environmentally harmful gases.

[1] Rémi Vallat, "Break healing and LER mitigation for low dose EUV exposure," in *AVS 69th , November 5-10,*(AVS 69th, Portland, OR, 2023).

[2] A. Fathzadeh, *J. Vac. Sci. Technol. A* 42, 033006 (2024), https://doi.org/10.1116/6.0003380

Author Index

Bold page numbers indicate presenter

— A —
Arvind, S.: PS1-MoM-5, **1**
— B —
Bezard, P.: PS1-MoM-5, 1
BEZARD, P.: PS1-MoM-11, **3**
Bézard, P.: PS1-MoM-6, 2
— C —
Chowdhury, R.: PS1-MoM-8, 2
Chowrira, B.: PS1-MoM-6, 2
— D —
De Gendt, S.: PS1-MoM-11, 3; PS1-MoM-5, 1
— F —
Fathzadeh, A.: PS1-MoM-11, 3; PS1-MoM-6, 2
Filippidou, K.: PS1-MoM-11, 3; PS1-MoM-6, 2
— G —
Gallagher, E.: PS1-MoM-11, 3
— H —
Holsteyns, F.: PS1-MoM-11, 3
— I —
Izawa, M.: PS1-MoM-3, **1**
— J —
Jang, S.: PS1-MoM-8, **2**
Joy, N.: PS1-MoM-2, 1
— K —
Katakam, S.: PS1-MoM-2, **1**
Kuwahara, K.: PS1-MoM-1, 1
— L —
Lee, J.: PS1-MoM-2, 1
— M —
Matsui, M.: PS1-MoM-1, **1**
Mignot, Y.: PS1-MoM-2, 1
Miura, M.: PS1-MoM-1, 1
Motoyama, K.: PS1-MoM-2, 1
— O —
Otto IV, I.: PS1-MoM-10, **2**
— P —
Park, C.: PS1-MoM-2, 1
Penny, C.: PS1-MoM-2, 1
Petersen, J.: PS1-MoM-5, 1
Poché, T.: PS1-MoM-8, 2
— R —
Ronse, K.: PS1-MoM-6, 2
— S —
Santos, D.: PS1-MoM-7, **2**
Shobha, H.: PS1-MoM-2, 1
Souriau, L.: PS1-MoM-6, 2
— T —
Tesfamariam, Y.: PS1-MoM-8, 2
— V —
Vallat, R.: PS1-MoM-11, 3; PS1-MoM-6, **2**
Vallee, C.: PS1-MoM-7, 2
Vallée, C.: PS1-MoM-10, 2
— W —
Witting Larsen, E.: PS1-MoM-5, 1
— Y —
Yan, D.: PS1-MoM-2, 1