CHIPS Act Mini-Symposium
Room C120-122 - Session CPS+CA-WeA

CHIPS Act: Interfaces and Defects

Moderators: Tina Kaarsberg, U.S. Department of Energy, Advanced Manufacturing Office, **Andrei Kolmakov**, National Institute of Standards and Technology (NIST)

2:20pm **CPS+CA-WeA-1 Future Needs and Current Trends in Interfacial Metrology for the Development of Reliable Ultra-Wide Bandgap Electronics**, ***Luke Yates***, *A. Jarzembski, W. Hodges, M. Bahr, W. Delmas, Z. Piontkowski, A. McDonald, M. Smith, B. Rummel, C. Glaser, A. Binder, J. Steinfeldt, A. Allerman, A. Armstrong, B. Klein, G. Pickrell,* Sandia National Laboratories*; D. Morisette,* Purdue University*; J. Cooper,* Sonrisa Research Inc.*; R. Kaplar,* Sandia National Laboratories **INVITED**

Recent advancements in epitaxial growth and substrate development continue to inspire the next generation of wide-bandgap (WBG) semiconductor devices. In the last decade, the silicon carbide (SiC) and gallium nitride (GaN) material systems have seen extraordinary advancements that allow an increased commercial device adaptation. However, there still exists many reliability concerns that directly impact device manufacturing. These concerns manifest in our inability to accurately quantify and mitigate interface charge effects and material defects that exist within device structures due to growth conditions and processing limitations. Commercial endeavors will continue to address such concerns for WBG devices, but it is crucial that the research community complements and promotes these efforts through advanced interfacial metrology methods that can be applied to both current WBG devices and future ultra-wide-bandgap (UWBG, $E_g > 3.4$eV) materials and devices, thus enabling the next leap forward in electronic device performance. These include materials such as high-Al-content AlGaN/AlN, Ga_2O_3, cubic BN, diamond, and others. Due to device performance scaling approximately as E_g^6, there exists substantial potential that has yet to be fully embraced in UWBG devices.

Interfacial metrology is a broad topic area that encompasses numerous thermal, mechanical, chemical, optical, and electronic properties at (dis)similar material interfaces. It is inextricably linked to our ability to develop devices that fully exploit the electronic capabilities of a given material system. This talk discusses current optical, acoustic, and electrical characterization efforts at Sandia and within the broader community to visualize and quantify interfacial properties, defects, and undesirable electronic charges within (U)WBG materials and devices. Specifically, a coupled hyper-spectral frequency-domain thermoreflectance/laser doppler vibrometry (FDTR/LDV) system that allows for enhanced understanding of thermal/mechanical properties of buried interfaces with a sensing depth greater than standard FDTR approaches has been implemented. Additionally, an improved quasi-static capacitance analysis method has been developed to more accurately evaluate interface traps at dielectric/(U)WBG material interfaces. Direct optical and photoemission approaches are becoming increasingly difficult to effectively utilize as larger bandgap devices are developed, necessitating the need for advanced thermal, vibrational, and electronic analysis methods. Future interfacial metrology efforts will require non-destructive methods that are capable of highly resolved in-situ full-field monitoring of buried interfaces within a device.

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3:00pm **CPS+CA-WeA-3 Diamond/h-BN Heterostructures for High-Performance Electronics**, ***Yamaguchi Takahide***, National Institute for Materials Science, Japan **INVITED**

Diamond is an ultra-wide bandgap semiconductor displaying a high breakdown electric field, high thermal conductivity, and high carrier mobilities. These intrinsic properties are suitable for creating power conversion and communications devices. In order to utilize its full potential, however, the properties of its surfaces and interfaces to other materials used in combination are important. Hydrogen-terminated diamonds (diamonds with their surface carbon atoms covalently bonded with hydrogen atoms) are widely used to make field-effect transistors (FETs). They show p-type surface conductivity even when the diamonds are not doped intentionally. The surface conductivity is attributed to surface transfer doping; electrons in the valence band of diamond are transferred to acceptors in an adjacent coating material, thereby forming holes in the diamond surface. The acceptor material includes adsorbed water, NO_2 gas, and oxides such as Al_2O_3, MoO_3, and V_2O_5, and coating the diamond surface with an acceptor material has been thought to be necessary to generate the surface conductivity. However, the surface transfer doping is accompanied by negatively charged acceptors, which cause carrier scattering and reduce hole mobility. It also leads to normally-ON operation, a finite conductivity at zero gate bias, which is undesirable particularly in power electronics.

In this presentation, I will present current trends in diamond electronics and our recent work on the creation of high-performance hydrogen-terminated diamond FETs without surface transfer doping [1]. We transferred a cleaved single crystal of hexagonal boron nitride (h-BN) on hydrogen-terminated diamond and used it as a gate insulator. This is useful for avoiding the formation of defects, which occurs in conventional deposition techniques and can cause acceptor states [2]. In addition, the transfer was made without exposing the diamond surface to air, using a vacuum suitcase and an Ar-filled glove box, which reduced the density of atmospheric acceptors. Our FETs exhibited excellent ON-state characteristics such as a room-temperature mobility of 680 $cm^2V^{-1}s^{-1}$, sheet resistance of 1.4 kΩ and gate-length-normalized ON current of 1600 µm mA mm^{-1}. These are among the best among p-channel wide-bandgap FETs. The FETs also exhibited normally OFF behavior with an ON/OFF ratio of 10^8. Our new approach for making diamond FETs could lead to the development of high-performance wide-bandgap p-channel devices for power electronics and communications.

[1] Sasama et al. Nature Electronics **5**, 37 (2022).

[2] Sasama et al. APL Materials **6**, 111105 (2018); Phys. Rev. Materials **3**, 121601(R) (2019); J. Appl. Phys. **127**, 185707 (2020).

4:20pm **CPS+CA-WeA-7 Hydrogenation of a $Cu_{2-x}O$ Confined Under Hexagonal Boron Nitride**, ***J. Trey Diulus***, *E. Strelcov,* NIST Center for Nanoscale Science and Technology*; Z. Novotny,* Empa (Swiss Federal Laboratories for Materials Science and Technology), Switzerland*; N. Comini,* University of Zurich, Switzerland*; A. Naclerio, P. Kidambi,* Vanderbilt University*; J. Osterwalder,* University of Zurich*; A. Kolmakov,* NIST Center for Nanoscale Science and Technology

Hexagonal boron nitride (h-BN) exhibits a wide array of unique chemical and electrical properties that presents itself useful in numerous applications, such as a gate dielectric for high mobility diamond transistors,[1] increasing corrosion resistance,[2] or a device encapsulating material.[3] h-BN can be epitaxially grown by chemical vapor deposition (CVD) on copper surfaces with any orientation, and a near perfect lattice match on the Cu(111) surface, making Cu an ideal substrate to study intercalation.[4,5] Intercalation of O_2 through h-BN to monitor oxidation of the Cu substrate can be studied during exposure to near ambient oxygen partial pressures (1-100 Pa),[6] or following exposure to atmosphere.[5] The oxidation occurs predominately at defects and/or grain boundaries in the h-BN, and occurs even at room temperature if the pressure is high enough (atm pressure), leading to a lifetime of a few weeks at these conditions for use of pristine unoxidized h-BN/Cu heterostructures.[5] To better understand this intercalation behavior, we studied the intercalation of H_2 to observe the extent of recovery of the original metallic surface/interface after the h–BN/$Cu_{2-x}O$ interface is formed. Using polycrystalline Cu foils with CVD grown h-BN after exposure to atmosphere for ~1 month as a model system, we assessed the reduction of the surface via two hydrogenation methods: (i) simple H_2 exposure of 10 Pa followed by annealing in vacuum (sequentially) and during H_2 exposure (simultaneously) (ii) exposure to a low power (75 W) H_2 remote plasma also using 10 Pa, allowing for H radicals to interact with the surface. With *in situ* x-ray photoelectron (XPS) and Auger electron spectroscopy (AES), we track the changes in surface chemistry following each hydrogenation attempt. Additionally, *in situ* scanning electron microscopy provides morphological maps of the foil surface. To further study this hydrogenation mechanism from a fundamental perspective, we utilized h-BN grown on single crystalline Cu(111) and collected *in situ* ambient pressure XPS for the reduction of an ordered cuprous oxide confined beneath h-BN. Ultimately, H-radicals and ions can attack the confined oxide and partially reduce the surface, yet we were unable to fully recover metallic Cu. Our results indicate the original metallic interface might be repaired without damaging the overlaying h-BN, which is of practical importance for development of h-BN encapsulated devices and interfaces.

[1]Sasama, Y. *et al. APL Mater* **6** (2018)

[2]Li, L. H. *et al. Adv Mater Interfaces* **1** (2014)

[3]Lo, C.-L. *et al. J Appl Phys* **128** (2020)

[4]Naclerio, A. E. *et al. Adv Mater*, 2207374 (2022)

[5]Kidambi, P. R. *et al. Chem Mater* **26**, 6380-6392 (2014)

[6]Diulus, J. T. *et al.* Towards 2D-confined catalysis on oxide surfaces. *ACS Nano* **Submitted** (2023)

4:40pm **CPS+CA-WeA-8 A Proven Model for Workforce Development**, ***David Ruzic***, *D. Andruczyk,* University of Illinois at Urbana-Champaign

At the University of Illinois at Urbana-Champaign we have set up two complimentary structures to enable workforce development in the field of semiconductor manufacturing. The first is a relatively new degree program, a "Masters of Engineering in Plasma Engineering". This is a non-thesis master's degree which specializes in plasma technology and science related to making the machines which make the chips. The flagship class is a plasma laboratory where the students operate and analyze the experiments themselves in Vacuum Technology, DC Plasmas, RF Plasmas, Langmuir Probes, Spectroscopy, Plasma Etching, Plasma PVD Deposition, Atmospheric Pressure Plasmas and Fusion Plasmas. The program can usually be finished in three semesters and is open to students from all fields of engineering and science.

This program can be coupled with sponsored research at the University, particularly through the Illinois Plasma Institute. Companies who are sponsoring research at Illinois can use the Masters program to recruit, retain or re-train employees. In the case of a current employee, that person goes to Illinois while still working for the company, perhaps being paid less than 100%. Their work role at Illinois is to help work on the research project that in being sponsored, and do other remote work. Their school role is to take the courses in the degree program which includes classes directly related to their work for the company itself. If the company pays for the tuition, the student is required to continue working for the company upon graduation for a limited time, or pay back the tuition. The company is ensured a better-trained more-educated employee. The student is ensured of a job.

Examples will be described, and a program outlined that could be set-up at any major University.

5:00pm **CPS+CA-WeA-9 Characterization of Buffer Layers for Remote Plasma-Enhanced Chemical Vapor Deposition of Germanium-Tin Epitaxial Layers**, ***Bridget Rogers***, Vanderbilt University; *S. Zollner, C. Armenta,* New Mexico State University; *G. Grzybowski,* KBR; *B. Claflin,* Air Force Research Lab

Germanium-tin alloys are of interest for infrared light detectors and lasers to increase capabilities in image and data capture and transmission, because they can have a direct band gap with more than about 7% tin. Remote plasma-enhanced chemical vapor deposition (PE-CVD) is particularly attractive for growth of Ge-Sn alloys because it enables low-temperature epitaxy directly on Si using common precursors GeH_4 and $SnCl_4$. The growth of such epilayers can be optimized with an initial high-temperature buffer layer. This presentation will focus on the characterization of this buffer layer using atomic force microscopy, ellipsometry, thin-film powder x-ray diffraction, and x-ray photoelectron spectroscopy (XPS) for different growth conditions.

Thin Ge and Ge-Sn buffer layers with 10-20 nm thickness were deposited on Si (100) substrates for one minute at temperatures from 360°C to 500°C varying the $SnCl_4$ flow. Ellipsometry spectra for all films show critical point structures in the E--$_1$, $E_1+\Delta_1$, and E_2 region of Ge, indicating that all layers are crystalline. A layer grown at 360°C without $SnCl_4$ is well described as an 11 nm thick layer of crystalline germanium with 2 nm of roughness. Adding $SnCl_4$ to the gas flow significantly reduces the height of the ε_2 maximum at E_2, indicating that the layer is rough. In addition, a new broad peak appears near 1.3 eV, which is attributed to plasmonic effects arising from metallic β-tin inclusions. The plasmon peak disappears in the layers grown at 490°C with the same $SnCl_4$ flow. We conclude that depositing the buffer layer with $SnCl_4$ at low temperatures leads to β-Sn precipitates, where plasmon oscillations can be excited, which are not present for high-temperature growth.

The tin contents in the layers were also estimated by x-ray photoelectron spectroscopy. While XPS measures the total amount of tin in the layers, the presence of substitutional tin in $Ge_{1-x}Sn_x$ alloy buffers is best determined with x-ray diffraction. The (002) diffraction peak is absent in our buffers grown without $SnCl_4$ or at high temperature. The (004) XRD peak position in these layers is also very similar to pure Ge. The $Ge_{1-x}Sn_x$ (002) peak does appear in buffers grown at temperatures lower than 460°C. From the position of the (004) XRD peak, we estimate the tin content to be below 7%. Tin content determined from XRD shifts is much lower than the total tin content of about 20% estimated by XPS.

In summary, the substitutional tin content in thin $Ge_{1-x}Sn_x$ buffer layers grown by PE-CVD is modulated by temperature and $SnCl_4$ flow rates. Excess tin is present in β-tin precipitates, which lead to plasmonic resonances in ellipsometry spectra.

5:20pm **CPS+CA-WeA-10 Comparative Study of Mechanical and Corrosion Behaviors on Heat Treated Steel Alloys**, ***Moe Rabea***, California State Polytechnic University, Pomona

This research examines the effects of heat treatment processes on the mechanical properties and corrosion resistance of 1045 and 4140 Steel Alloys for industrial applications. Heat treatment processes of full annealing, normalizing, quenching, and tempering are carried out on the alloy samples. The mechanical and corrosion resistance tests of the heat treated samples are carried out and the results obtained are related to their morphologies analysis. The results show that the heat treatment processes have an effect on the tensile strength, impact, and a significant effect on the corrosion resistance of the alloy samples. With respect to the strain characteristics, significant improvement in the ductility of the samples is recorded in the full annealing and alloy tempered samples. Thus, for application requiring strength and ductility such as in aerospace industries, this tempered heat treated alloy could be used. In addition, the quenched sample shows a significant improvement in hardness.

CHIPS Act Mini-Symposium
Room C120-122 - Session CPS+MS-ThM

Chips and Science Act Implementation for Microelectronics (Including Workforce)

Moderators: Alain Diebold, SUNY Polytechnic Institute, **Tina Kaarsberg**, U.S. Department of Energy, Advanced Manufacturing Office

8:00am **CPS+MS-ThM-1 The Goals for the CHIPS and Science Act of 2022**, *D. Lavan,* ***Jay Lewis,*** National Institute for Science and Technology (NIST) **INVITED**

The goals for the CHIPS and Science Act of 2022 are to strengthen American manufacturing, supply chains, and national security, and invest in research and development, science and technology, and the workforce of the future to keep the United States the leader in the industries of tomorrow, including nanotechnology, clean energy, quantum computing, and artificial intelligence. An update on progress implementing the CHIPS and Science act will be provided, focusing on R&D Programs including the NSTC, the NAPMP, Manufacturing USA and the Metrology Program.

8:40am **CPS+MS-ThM-3 U.S. CHIPS Act and Semiconductor R&D Centers: Accelerating American Innovation**, ***David Anderson,*** NY CREATES **INVITED**

This presentation by David Anderson, President of the New York Center for Research, Economic Advancement, Technology, Engineering, and Science (NY CREATES), details the latest updates on the U.S. CHIPS and Science Act and discusses semiconductor R&D centers as key drivers for stimulating innovation, enhancing domestic chip manufacturing capabilities, and bolstering the United States' position in the global semiconductor industry. Through an analysis of the CHIPS Act's key components and the vision put forth by the Federal government, Mr. Anderson will highlight its unprecedented opportunities for accelerating semiconductor R&D and cultivating a robust ecosystem within the U.S. Additionally, this presentation showcases the pivotal role of semiconductor R&D centers in harnessing collaborative research efforts, fostering public-private partnerships, and nurturing talent. Drawing upon his decades of experience in the industry, Anderson demonstrates the positive impact of semiconductor R&D centers on industry growth, job creation, and national security. Attendees will gain insights into the innovative research initiatives, cross-sector collaborations, and technology roadmaps that these centers facilitate, and how the CHIPS Act will help to propel the U.S. to the forefront of the semiconductor industry.

9:20am **CPS+MS-ThM-5 A View on the 1000x Performance Efficiency Goal**, ***Steve Pawlowski,*** Intel **INVITED**

Over the last two decades, large HPC machine efforts have become a procurement exercise. A large set of applications have been unable to leverage the additional computational power of newly-procured machines without significant additional software development. The machine architectures need to evolve: new systems architectures and innovations require a deep understanding of application uses cases and their needs. Memory and storage, as foundational elements, will be at the center of future innovative systems, driving both greater performance and increased energy efficiency. We have a performance efficiency goal of achieving 1000x over the next 20 years. This talk posits that $\geq$100x of the 1000x gain can be realized through repartitioning/packaging changes. The <10x that remains can come from re-architecting the system based on a detailed understanding of the targeted applications.

11:00am **CPS+MS-ThM-10 Re-Shoring and Re-Energizing Microelectronics: the Workforce Challenge**, *M. Lundstrom,* ***Vijay Raghunathan,*** Purdue University **INVITED**

The CHIPS and Science Act is a bold initiative designed to re-shore semiconductor manufacturing, secure our supply chain, re-gain the lead in leading-edge chip technology, bolster our leading positions in design and semiconductor manufacturing equipment, and accelerate the pace of innovation. Accomplishing these ambitious objectives will require the kinds of mission-driven, deep university-industry-government partnerships that we have not seen since the Manhattan Project and Space Race. The semiconductor workforce is a key challenge – not just a larger workforce, but one educated to advance electronics in the new era we are entering. This talk will present the author's perspective on the magnitude of the challenge, the intimate connection between research, teaching, and innovation that must be maintained, the educational needs for new era electronics, how companies and universities should work together, and the role of international partnerships.

11:40am **CPS+MS-ThM-12 Saving Power with New Designs and Chiplets in the New Era of Advanced Packaging**, ***Jan Vardaman,*** TechSearch International, Inc. **INVITED**

Energy saving through new designs and package architectures including chiplets are driving developments and options in high-performance computing. An increasing number of companies are turning to chiplets, not only to achieve the economic advantages lost with expensive monolithic scaling, but also to meet the power savings requirements for datacenters and other high-performance computing applications. Co-packaged optics holds promise and is under development by a number of companies. Design with chiplets is one approach under consideration.. A chiplet is not a package, but it is a new approach to system, package, and chip design. There are many package options that can be adopted and careful consideration is required to select the most appropriate options for the application. Options include the emerging 3DIC format with mircobumps or hybrid bonding, laminate substrate package, fan-out on substrate, and silicon interposer. Challenges include design, test, assembly, and thermal. This presentation focuses on the move to energy savings and design and package methods being introduced to achieve power and performance goals.

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