Single-nm-resolution Gate Fabrication for Top-Gated Quantum Dot Qubits

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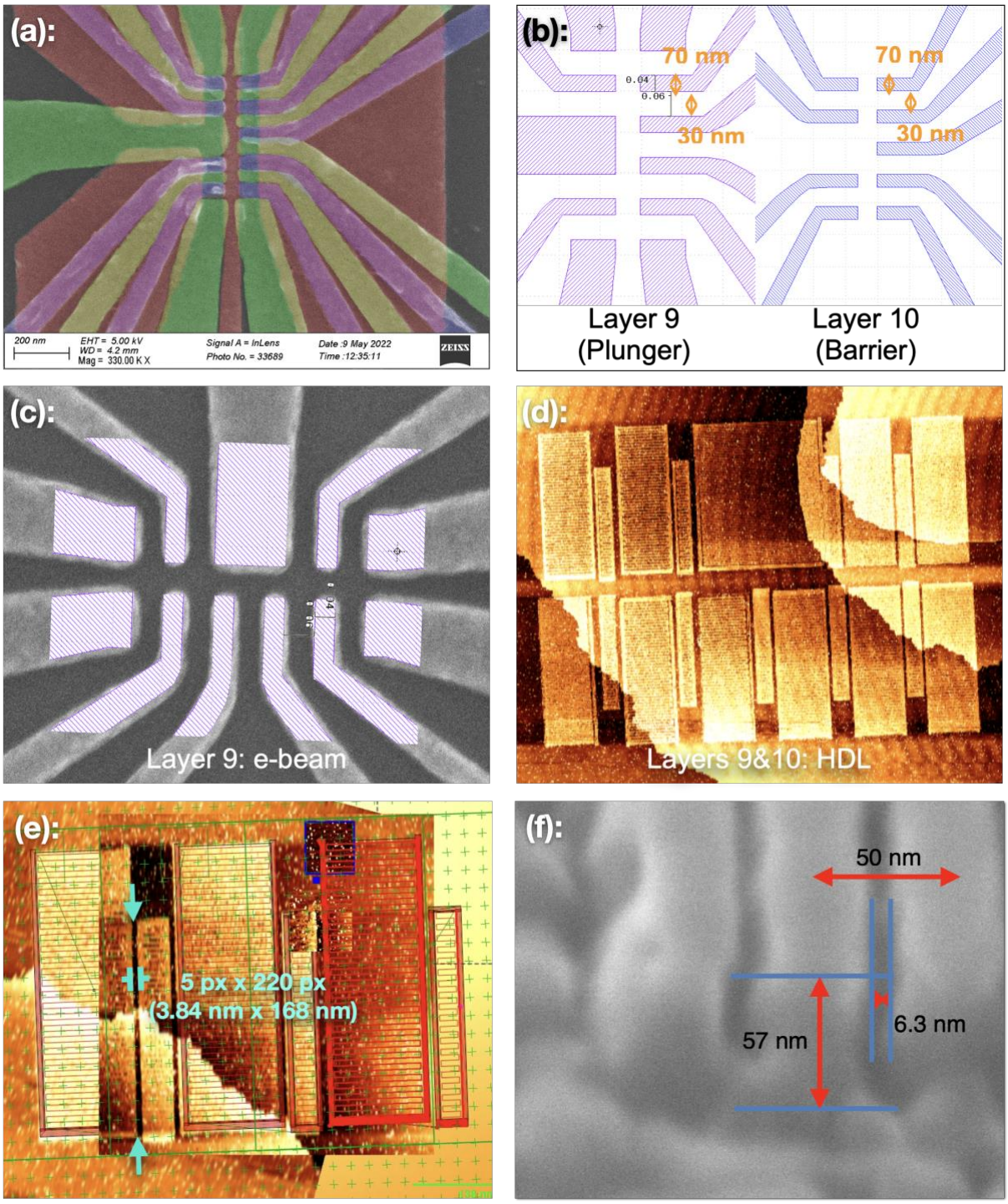

Figure 1. (a): Gate-defined Quantum Dot qubit fabricated using e-beam lithography. Plunger gates are shown in green, barrier gates in purple. (b): Due to imprecision in the e-beam lithography, the two sets of gates are patterned in two layers, 9 & 10. (c): Result vs. the pattern for layer 9 shows the imprecision in the gate dimensions using e-beam lithography. (d): With HDL, by contrast, we can write the patterns for both layers 9&10 in one step. (e): The HDL gate patterns have much higher precision, with gaps of 4 nm or less 160 nm long, and errors of 1 nm or less. (f): Test nanoimprint template after AS-ALD and RIE. A gap of 6.3 nm for a 57 nm high structure was fabricated, but some edge precision has been lost.