Atomic Scale Processing Mini-Symposium
Room A107-109 - Session AP2+PS+TF-TuA

Energy Enhanced ALD

Moderator: John F. Conley, Jr., Oregon State University

5:00pm **AP2+PS+TF-TuA-9 Atomic Layer Annealing with Radio Frequency Substrate Bias for Control of Grain Morphology in Gallium Nitride Thin Films**, *A. Mcleod, P. Lee,* University of California, San Diego*; S. Yun, S. Ueda,* University of California, San Diego, USA*; Z. Devereaux, C. Winter,* Wayne State University*; J. Spiegelman,* RASIRC*; R. Kanjolia, M. Moinpour,* EMD Electronics, USA*;* ***Andrew Kummel****,* University of California, San Diego **INVITED**

Low temperature GaN deposition is critical for passivation layers on nitride power FET as low as templating and capping layers on sputtered AlN films for heat spreader. A method of performing atomic layer annealing with RF substrate bias on insulating and amorphous substrates is demonstrated for GaN deposition at 275 ℃. GaN is typically deposited by MOCVD or MBE at >600 ℃, resulting in strain upon cooling; this makes low temperature process alternatives desirable. Tris(dimethylamido) gallium (III) and hydrazine served as precursors while Ar and Kr were used for ion bombardment. Optimization of substrate bias potential is demonstrated by GI-XRD and XRR. Reference films were deposited by thermal ALD and non-substrate biased ALA processes. XPS surface and depth-profiling studies show that applied RF bias decreases film oxygen and carbon content relative to the reference films; these films also show crystallites broadening with increasing film thickness by TEM in contrast to the reference films. In summary, ALA with RF substrate bias is demonstrated as an effective method to deposit GaN thin films at a low deposition temperature on insulators.This technique has recently been expended to growth of InGaN films which applications in microLEDs.

5:40pm **AP2+PS+TF-TuA-11 Atomic Layer Annealing for sub-10 nm, Wake-up Free Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Thin Films**, ***Yu-Sen Jiang****,* National Taiwan University, Taiwan*; T. Chang, S. Yi,* Taiwan Semiconductor Manufacturing Company, Taiwan*; M. Chen,* National Taiwan University, Taiwan

Conventional annealing techniques pose significant challenges in nanoscale fabrication. One prominent issue involves the heating depth, which typically exceeds the critical dimension of nanoscale devices. Consequently, conventional annealing methods introduce excessive thermal budget, resulting in performance degradation of the devices. Atomic layer annealing (ALA) is capable of adjusting the film quality at the atomic level during low-temperature (300℃) deposition without the need for any post-annealing process, which tremendously lowers the thermal budget and can tailor the film properties as required. In this report, the ALA technique was used to realize sub-10 nm wake-up free ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) thin films with high remnant polarization and low thermal budget. The HZO thin films have also been used as gate dielectrics in junctionless transistors, demonstrating steep subthreshold swing (< 60 mV/decade) in nanoscale devices. The outcome manifests the remarkable capabilities of ALA in enabling precise engineering and fabrication of nanoscale materials and devices.

6:00pm **AP2+PS+TF-TuA-12 A System for Predicting the Area Selective Deposition of Titanium: Plasma State Diagnostics Using Electrical Simulation**, ***Kyoungmi Choi****, T. Hong, H. Kim, Y. Oh,* Samsung Electronics Co., Inc., Republic of Korea

The selective deposition of thin films in specific areas is crucial for achieving the desired size and lowresistance of semiconductors. Due to differences in chemistry between molecule/surface and molecule/vapor interactions, thin films are selectively deposited on pre-patterned substrates. Although simulations have been used to predict Ti film thickness using plasma simulation and surface reaction models, the effect of selective deposition on the pattern was not studied. In this study, an electrical simulation was used to predict the selectivity of the area selective deposition process on the patterned wafer.

To identify the main factors affecting selectivity, we reviewed the plasma temperature and density. Plasma density can be indirectly inferred from the output current of the matcher. Another factor that influences selectivity is plasma temperature, specifically the electron temperature [eV]. The sheath voltage is proportional to the electron temperature. Therefore, we established an electric simulation system (Fig. 1) to estimate the sheath voltage. The CCP consists of an RF generator, a matcher, and a chamber. We identified the matcher parameters (C_{tune}/C_{load}/L) using the maximum power transmission theory, assuming that the chamber was $Z_{chamber}$(Fig 2). The model was verified using MATLAB and the sheath voltage was derived using the matcher and bottom currents. The simulations and evaluations of pressure/RF power/impedance were performed. The validity of the electrical model was confirmed by comparing the simulation and the experimental current.

To verify the simulation, Ti deposition experiments were conducted on Si/SiO wafers under 7 conditions (Table1). The simulation results for sheath voltage and the experimental results for deposition rate showed a correlation of 0.77, and the Si/SiO selectivity showed a correlation of 0.92(Fig 3).

Through the correlation result,itwasderivedasthefollowingconclusion.The correlation results between sheath voltage and the area selective deposition explains the difference in the activation energy of the Si/SiO surfaces: The Si-Si bonding energy is 3.39 eV and the Si-O bonding energy is 8.29eV (Fig 4). Since there are regions where the plasma temperature is active on Si and inert on SiO, they are selectively deposited. Therefore, a sheath voltage simulation can be used to predict the selectivity. With further development, this simulation can be applied to other deposition equipment that uses plasma, and trends in process results for other process parameters that are sensitive to plasma temperature can be inferred.

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