CHIPS Act Mini-Symposium
Room C120-122 - Session CPS+MS-ThM

Chips and Science Act Implementation for Microelectronics (Including Workforce)

Moderators: Alain Diebold, SUNY Polytechnic Institute, **Tina Kaarsberg**, U.S. Department of Energy, Advanced Manufacturing Office

8:00am **CPS+MS-ThM-1 The Goals for the CHIPS and Science Act of 2022**, *D. Lavan,* ***Jay Lewis,*** National Institute for Science and Technology (NIST) **INVITED**

The goals for the CHIPS and Science Act of 2022 are to strengthen American manufacturing, supply chains, and national security, and invest in research and development, science and technology, and the workforce of the future to keep the United States the leader in the industries of tomorrow, including nanotechnology, clean energy, quantum computing, and artificial intelligence. An update on progress implementing the CHIPS and Science act will be provided, focusing on R&D Programs including the NSTC, the NAPMP, Manufacturing USA and the Metrology Program.

8:40am **CPS+MS-ThM-3 U.S. CHIPS Act and Semiconductor R&D Centers: Accelerating American Innovation**, ***David Anderson,*** NY CREATES **INVITED**

This presentation by David Anderson, President of the New York Center for Research, Economic Advancement, Technology, Engineering, and Science (NY CREATES), details the latest updates on the U.S. CHIPS and Science Act and discusses semiconductor R&D centers as key drivers for stimulating innovation, enhancing domestic chip manufacturing capabilities, and bolstering the United States' position in the global semiconductor industry. Through an analysis of the CHIPS Act's key components and the vision put forth by the Federal government, Mr. Anderson will highlight its unprecedented opportunities for accelerating semiconductor R&D and cultivating a robust ecosystem within the U.S. Additionally, this presentation showcases the pivotal role of semiconductor R&D centers in harnessing collaborative research efforts, fostering public-private partnerships, and nurturing talent. Drawing upon his decades of experience in the industry, Anderson demonstrates the positive impact of semiconductor R&D centers on industry growth, job creation, and national security. Attendees will gain insights into the innovative research initiatives, cross-sector collaborations, and technology roadmaps that these centers facilitate, and how the CHIPS Act will help to propel the U.S. to the forefront of the semiconductor industry.

9:20am **CPS+MS-ThM-5 A View on the 1000x Performance Efficiency Goal**, ***Steve Pawlowski,*** Intel **INVITED**

Over the last two decades, large HPC machine efforts have become a procurement exercise. A large set of applications have been unable to leverage the additional computational power of newly-procured machines without significant additional software development. The machine architectures need to evolve: new systems architectures and innovations require a deep understanding of application uses cases and their needs. Memory and storage, as foundational elements, will be at the center of future innovative systems, driving both greater performance and increased energy efficiency. We have a performance efficiency goal of achieving 1000x over the next 20 years. This talk posits that $\geq$100x of the 1000x gain can be realized through repartitioning/packaging changes. The <10x that remains can come from re-architecting the system based on a detailed understanding of the targeted applications.

11:00am **CPS+MS-ThM-10 Re-Shoring and Re-Energizing Microelectronics: the Workforce Challenge**, *M. Lundstrom,* ***Vijay Raghunathan,*** Purdue University **INVITED**

The CHIPS and Science Act is a bold initiative designed to re-shore semiconductor manufacturing, secure our supply chain, re-gain the lead in leading-edge chip technology, bolster our leading positions in design and semiconductor manufacturing equipment, and accelerate the pace of innovation. Accomplishing these ambitious objectives will require the kinds of mission-driven, deep university-industry-government partnerships that we have not seen since the Manhattan Project and Space Race. The semiconductor workforce is a key challenge – not just a larger workforce, but one educated to advance electronics in the new era we are entering. This talk will present the author’s perspective on the magnitude of the challenge, the intimate connection between research, teaching, and innovation that must be maintained, the educational needs for new era electronics, how companies and universities should work together, and the role of international partnerships.

11:40am **CPS+MS-ThM-12 Saving Power with New Designs and Chiplets in the New Era of Advanced Packaging**, ***Jan Vardaman,*** TechSearch International, Inc. **INVITED**

Energy saving through new designs and package architectures including chiplets are driving developments and options in high-performance computing. An increasing number of companies are turning to chiplets, not only to achieve the economic advantages lost with expensive monolithic scaling, but also to meet the power savings requirements for datacenters and other high-performance computing applications. Co-packaged optics holds promise and is under development by a number of companies. Design with chiplets is one approach under consideration.. A chiplet is not a package, but it is a new approach to system, package, and chip design. There are many package options that can be adopted and careful consideration is required to select the most appropriate options for the application. Options include the emerging 3DIC format with mircobumps or hybrid bonding, laminate substrate package, fan-out on substrate, and silicon interposer. Challenges include design, test, assembly, and thermal. This presentation focuses on the move to energy savings and design and package methods being introduced to achieve power and performance goals.

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