Manufacturing Science and Technology Group
Room C120-122 - Session MS-FrM

Microelectronics R&D for Life-Cycle Energy Efficiency

Moderators: Nicholas Johnson, Energetics, **Tina Kaarsberg**, U.S. Department of Energy, Advanced Manufacturing Office

8:20am **MS-FrM-1 Energy Efficient Scaling in Microelectronics: Enabling a New Era in Computing for a Sustainable Future***, **Sadasivan Shankar**,* SLAC National Accelerator Laboratory **INVITED**

The geometrical scaling of integrated circuit technology (known by the moniker as Moore's law) has led to many of the computing-based innovations over the last half century. Given the slowing down of scaling, it is important that the energy efficiency of computing should increase to offset the increasing number of digital devices and growing ubiquity of computing in all aspects of the world economy. To understand energy limits for information processing, we explore energy associated with both human-made and natural systems.

Based on lessons from the nature and fundamental analysis, we propose a new paradigm is to double the energy efficiency of computation in every succeeding generation in addition to the ongoing technological scaling. Using examples of synapses from a mammalian brain and quantum information, we estimate the headroom available for energy reduction to be of the order of 1000X to a million or more depending on the metrics. This can be enabled by trade-offs of the performance at the single switch level, with that at the system level including communication and storage, and with the total compute operations needed at the application level.

The opportunities for this new trajectory in computing resides in combinations of architectures, materials, devices, and algorithms/software and application-specific information processing. This energy-based design and scaling in turn could lead to exponential use of computing in even more innovative ways from Artificial Intelligence-driven applications, driverless cars, and smart grids due to the resulting Rebound Effect.As computing is the foundation of new sustainable economy, the intent of this new era is to leverage innovations in science and technology to form a green framework for the planet.

9:00am **MS-FrM-3 Improving Asic Energy Efficiency from Systems to Silicon***, **Godwin Maben**,* Synopsys, Inc **INVITED**

Improving Energy efficiency while designing an electronic product, includes considering power as one of the constraints from the beginning of chip design, Macro Architecture selection, power performance trade-offs, appropriate workload selection, defining a power efficient architecture from Hardware perspective and designing an efficient Firmware, System's software , Application Software....etc.

In this presentation, we will look into every aspect of design cycle, in developing a complete platform, which is energy efficient from Systems to Silicon and How EDA tools have emerged as one of the key component in addressing Energy Efficiency, in addition to traditional Performance.

9:40am **MS-FrM-5 Atomic Precision Advanced Manufacturing for Tunnel Field Effect Transistors***, **Shashank Misra**,* Sandia National Laboratories **INVITED**

The energy efficiency of microsystems improved by more than 1000x every 20 years under Dennard scaling, where shrinking the linear dimension of a transistor while maintaining a constant electric field scaled the frequency and the voltage of operation. Satisfying the continued demand for computing, when scaling is projecting a single doubling of energy efficiency over the next 15 years, will require innovation across algorithms, architectures, and devices. Sandia has established programs pursuing the basic research underlying probabilistic neuromorphic computing, reconfigurable architectures, energy-efficient AI at the edge, and material manipulation for fine-grained integration of sensing and computation. In this talk, I will focus on a specific transistor that circumvents the physical limitation that ended Dennard scaling, and lowers the operating voltage of a circuit.

Tunnel field effect transistors (TFETs) rely on band-to-band tunneling, and promise a 10x improvement in energy efficiency compared to metal oxide semiconductor transistors (MOSFETs), all while maintaining the same materials. They have not achieved this promise due to poor on:off current ratios, and smeared dopant profiles producing gradual turn-on currents. We have designed a TFET in a vertical geometry which uses atomic precision advanced manufacturing (APAM) to form the buried electrode and the intrinsic tunnel barrier. This design boosts current by scaling with the area of the device instead of a 1D edge and obviates limitations from the abruptness of the doping profile. However, APAM has traditionally only been used to fabricate qubits, and has little to do with microelectronics.

Here, we integrate APAM with conventional fabrication, providing a straightforward path both to advanced transistor devices that work in practical conditions, and to scaled manufacturing. We first demonstrate both the two halves of the vertical TFET device operating at room temperature. We show an APAM nanowire integrated with common back end of line processing, which reveals the APAM nanowire strongly confines carriers, leading to current densities that exceed that of copper. Next, we demonstrate the gated top half the TFET device, limiting processing to thermal budgets tolerated by APAM. The low-thermal budget MOS transistor is used to evaluate the quality of APAM material. Next, we demonstrate integration into a CMOS fabrication flow, complete with working hybrid APAM-CMOS circuits. Finally, we explore operational robustness by showing that CMOS features fail before APAM features in accelerated lifetime testing.

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10:40am **MS-FrM-8 Materials, Devices, and Packaging Opportunities Towards a Super Energy Efficient Future***, **Paul Fischer**,* Intel Corp. **INVITED**

As highlighted in the SRC's decadal plan, the total energy consumption by microelectronics is doubling approximately every three years while the world's energy production is growing only linearly and at about 2% per year.Despite the efficiency gains from continued Moore's Law scaling, global hunger for compute is growing faster.At Intel we are committed to building a more Responsible, Inclusive, and Sustainable world Enabled by our collective actions and in 2020 laid out our RISE strategy and goals which include a 10x increase in product energy efficiency by 2030.

But what emerging technology options are in the research pipeline to enable product energy efficiency which could shape future opportunities consistent with the Department of Energy's Energy Efficiency Scaling over 2 decades (EES2) effort?Product energy consumption is ultimately the culmination of broad technology ingredients spanning applications, software, algorithms, architectures, circuits, materials, devices, and packaging.In this talk Dr. Fischer will discuss a subset of these ingredients best aligned with AVS conference themes: emerging materials, devices, and packaging technologies which could drastically alter the energy requirements of future microelectronic products.

11:20am **MS-FrM-10 EES2 Update—A Pledger's Perspective***, **Steve Pawlowski**,* Intel **INVITED**

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