

Quantum Science and Technology Mini-Symposium

Room B110-112 - Session QS-MoA

Systems and Devices for Quantum Computing

Moderators: Ekta Bhatia, NY CREATES, Dave Pappas, Rigetti Computing

1:40pm QS-MoA-1 Hole-Based, Atomic-Scale Quantum Devices in Silicon, Robert Butera, Laboratory for Physical Sciences

INVITED

δ -doped Si provides a novel frontier to explore quasi-2D electronic transport of an extremely high concentration of carriers ($> 10^{14} \text{ cm}^{-2}$) through a highly-disordered potential. These carriers can be further confined using atomic-precision advanced manufacturing (APAM) techniques to generate a variety of atomic-scale quantum devices [1]. Over the past two decades these techniques have been used to realize and characterize atomic-scale wires, single atom and single electron transistors, as well as single atom qubits based on P [2-5], the quintessential electron donor dopant for Si. In contrast, atomic-scale quantum devices have only recently begun to be explored with B [6, 7], the archetypal acceptor dopant in silicon.

Under standard conditions, a single B atom in Si has an associated hole that forms a promising single qubit platform on its own right [8], but with sufficiently high concentrations of B, Si has been shown to exhibit superconductivity [9]. Motivated by these intriguing possibilities, we developed an APAM-compatible process for B to ultimately explore single acceptor qubits and atomic-scale, superconducting Si devices. Here we discuss the fabrication and initial characterization of the resulting hole-based, atomic-scale quantum devices in which we observe weak anti-localization and universal conductance fluctuations in magnetotransport measurements, and demonstrate Coulomb oscillations in a single hole transistor.

[1] Bussmann, E., Butera, R.E., Owen, J.H.G. *et al.*, Atomic-precision advanced manufacturing for Si quantum computing. *MRS Bulletin* **46**, 607–615 (2021).

[2] B. Weber, S. Mahapatra, H. Ryu, *et al.*, Ohm's Law survives to the atomic scale. *Science* (2012).

[3] Fuechsle, M., Miwa, J., Mahapatra, S. *et al.*, A single-atom transistor. *Nature Nanotech* **7**, 242–246 (2012).

[4] Wang, X., Wyrick, J., Kashid, R. *et al.*, Atomic-scale control of tunneling in donor-based devices. *Commun Phys* **3**, 82 (2020).

[5] Y. He, S.K. Gorman, D. Keith, *et al.*, A two-qubit gate between phosphorus donor electrons in silicon. *Nature* (2019).

[6] K. Dwyer, S. Baek, A. Farzaneh, *et al.*, B-doped δ -Layers and nanowires from area-selective deposition of BCl_3 on Si(100) *ACS Appl. Mater. Interfaces*, **13** (34) (2021), pp. 41275–41286.

[7] Škerek, T.; Köster, S. A.; Douhard, B.; *et al.*, A. *Bipolar Device Fabrication Using a Scanning Tunneling Microscope*. *Nat. Electron* **2020**, *3*, 524–530.

[8] Kobayashi, T., Salfi, J., Chua, C. *et al.*, Engineering long spin coherence times of spin-orbit qubits in silicon. *Nat. Mater.* **20**, 38–42 (2021).

[9] Bustarret, E., Marcenat, C., Achatz, P. *et al.* Superconductivity in doped cubic silicon. *Nature* **444**, 465–468 (2006).

2:20pm QS-MoA-3 Interface Loss Engineering for High Coherence Aluminium Qubits, Janka Biznarova, J. Bylander, Chalmers University of Technology, Gothenburg, Sweden

Superconducting qubits are current hot candidates for delivering on the promise of quantum computation. However, their implementation is not without challenges. Quantum information stored in a qubit has a finite lifetime before it loses coherence. For superconducting qubits to be able to sustain the fragile quantum information in a coherent state sufficiently long so that a meaningful number of logical gates can be executed, it is vital to examine the sources of decoherence and to eliminate them. In this work, we show how improvements in device fabrication can enable T_1 times of up to 500 μs in aluminium-based transmon qubits.

The nature of the sources of coherence loss in quantum circuits is a topic of ongoing debate. In this work we investigate the parasitic two-level systems (TLS) that compete with our devices for photons, as well as uncover other losses that may limit performance once TLS loss has been mitigated.

This problem can be approached from two angles - through optimizing device geometry, and through surface engineering. Manipulating device geometry, we can quantify the relative effect each interface of the CPW resonator has on the total loss, and minimize the participation of the lossiest interfaces. With surface engineering, we can target a given interface in order to mitigate the specific type of loss it entails.

In this work, we design, fabricate and characterize resonators and qubits using aluminium on silicon in order to further investigate the nature of TLS. We vary the deposition conditions of the metal, as well as surface treatments, and draw conclusions for the participation of TLS loss to the total loss of the circuits at low temperatures. Varying the absolute size of the CPWs, as well as the ratio of the CPW center conductor to its gap to ground, we can get a more accurate picture of the various loss contributions. Once a fabrication recipe is optimized for a resonator proxy, the recipe is extended to qubit fabrication. We show that aluminium-based transmon qubits fabricated with the optimized recipe can reach T_1 values up to 500 μs , with mean T_1 values exceeding 200 μs .

2:40pm QS-MoA-4 Examine the Electrical Transport Properties of Superconducting Quantum Devices Based on PtSi, Tharangana Nanayakkara, A. Bollinger, R. Li, M. Liu, C. Black, Brookhaven National Laboratory

Quantum information systems have the potential to revolutionize many fields, including health, defense, and finance. Despite their vast potential, practical applications of quantum information systems face numerous challenges that must be addressed to fully realize their benefits. Fabricating nano-scaled superconducting qubits for quantum information systems is a highly challenging process. One of the primary remaining challenges is identifying suitable superconducting materials with sufficient coherence times in their qubits. Therefore, it is essential to investigate novel materials, such as platinum silicide (PtSi), to recognize their potential candidacy in quantum information science. PtSi is a transition metal silicide, formed by reacting silicon with platinum. PtSi finds extensive use in semiconductor microelectronics since its ability to create low resistance electrical contacts to silicon. Significantly, PtSi exhibits superconducting properties, and it is a potential material for integrating quantum computation with silicon technology.

In this study, Pt thin films were deposited onto silicon substrates using magnetron sputtering technique. Subsequently, the Pt on the silicon wafer was thermally annealed in a rapid thermal processor to form PtSi thin films, which were confirmed by X-ray diffraction measurements. We patterned PtSi thin films on Si substrate using electron-beam lithography to fabricate superconducting devices, including constriction type Josephson junctions (JJs), and Superconducting Quantum Interference Devices (SQUIDs). The fabrication process for constriction-type devices involves a single-step electron-beam lithography, which is simpler than the conventional tunneling junction fabrication process. After patterning the device structure onto the PtSi, a reactive ion etching technique was used to carve the device shape by selectively etching away the surrounding PtSi.

Monday Afternoon, November 6, 2023

We performed low-temperature electrical transport measurements on constriction type JJs and SQUIDs to evaluate the material characteristics for high-quality superconducting quantum circuit fabrication. The parameters extracted from the PtSi devices, including critical temperature, normal-state resistance, coherence length, critical current density, and critical field values, will be comprehensively discussed in this work.

3:00pm **QS-MoA-5 Two Architectures for Superconducting Quantum Processors with Tunable Couplers**, *Stefano Poletto*, Rigetti Computing
INVITED

Superconducting quantum processor units (QPUs) with 10s to 100s of physical qubits are now commercially available from multiple companies and institutions. However, to build and operate a high performance superconducting QPU several physics and engineering challenges must still be addressed.

In this talk, I will focus on the implementation of tunable qubit-qubit interactions as a promising alternative to fixed coupling schemes from both a scalability and performance point of view. I will present two types of floating tunable coupler architectures as well as two different methods to implement two-qubit gates. I show how floating tunable couplers allow increased physical separation between qubits; making it an ideal candidate for scalability. Additionally, the two-qubit parametric resonance gate can also help reduce the incoherent errors per operation by performing the gate at its maximum speed. I will give a side-by-side comparison of the different architectures to highlight the benefits of the proposed approaches.

4:00pm **QS-MoA-8 Quantum Device Formation in Silicon via Ion Implantation**, *Jeffrey McCallum*, School of Physics, Australia
INVITED

Spin qubits based on impurities such as phosphorus, P, in isotopically pure silicon ^{28}Si , have attractive attributes for development of quantum computing devices.[1] Very long coherence times can be achieved for donor-based qubits when the ^{29}Si atoms, that otherwise lead to decoherence, are removed from the active region of the device. Standard semiconductor-industry ion implantation techniques can be used to fabricate well-behaved donor qubits in Si. Exceptionally long coherence times greater than 30 s have been demonstrated for nuclear spin qubits. Conditional quantum operation of a pair of exchange coupled single P-donor spin qubits in an ion implanted ^{28}Si epi-layer device has also been recently demonstrated.[2] While many key achievements have been obtained for P donor qubits in Si, other donor qubit systems such as antimony, Sb, and bismuth, Bi, are also starting to be developed and have potential to offer new degrees of freedom and new qubit control functionalities. The crucial next stage is to develop suitable scale-up pathways that allow patterned arrays of donor qubits to be controllably coupled and that are robust against the inherent donor placement tolerances and material processing constraints that exist. Here, we will review progress on the fabrication and measurement of ion implanted donor-based qubits in silicon and discuss the pathway to deterministically implanted single donor arrays with inter-donor spacings suitable for available coupling protocols.

Silicon is also an attractive platform for the development of devices that contain both superconducting and semiconducting components on a single chip for emerging quantum technologies. Recently, we have investigated superconductivity in nanowire devices fabricated using an Al-Si exchange process in silicon-on-insulator wafers.[3] The Al-exchange-transformed material is conformal with predefined device patterns. Magneto-transport measurements on nanoring structures formed by this process exhibit periodic features in the differential resistance and in the critical current resulting from fluxoid quantization. The devices can be operated in temperature/magnetic-field regimes where some components of the device are in the superconducting state while others are in resistive states. The details of the Al-Si exchange process suggest that it could allow a range of new nanoscale superconducting-semiconducting device structures to be formed. Here, we will also briefly introduce our preliminary exploration of these superconducting nanowire devices and their promise for quantum technologies development.

[1] J. C. McCallum, et al., Appl. Phys. Rev. 8, 031314 (2021).

[2] M. T. Madzik, et al., Nat. Commun. 12, 181 (2021).

[3] B. C. Johnson, et al., Nano Lett. 23, 17–24, (2023).

4:40pm **QS-MoA-10 Quantum Technology Manufacturing Roadmap v1.0**, *Jonathan Felbinger*, SRI International

This roadmap effort, led by SRI International and its team of industry, national lab and academic partners, will identify pre-competitive
Monday Afternoon, November 6, 2023

development work and supply chain gaps to support scaling up quantum technology and help maintain U.S. dominance in quantum-related fields, rather than focus on scientific discovery or a specific application.

Quantum information science and technology are rapidly advancing and have potential applications in computing, sensing, communications and security. The development of quantum technology and a U.S.-based quantum industry is a key strategic priority of the U.S. government. To achieve its full potential, novel materials, devices, structures and systems must be developed and manufactured. Though still emerging, the quantum industry is taking shape, products are beginning to emerge and companies are developing internal roadmaps for more complex systems, such as error-corrected quantum computers.

To support the development of technology critical to the quantum industry, SRI and its team of industry, national lab and academic partners propose to develop a technology roadmap focused on supply chain gaps and barriers to advanced manufacturing capability. SRI currently manages the Quantum Economic Development Consortium [<https://quantumconsortium.org/>] (QED-C), an industry-led consortium supported by the U.S. government and 170+ industry, academic and national lab members. The mission of QED-C is to enable and grow the U.S. quantum industry and supply chain. SRI proposes to leverage ties with QED-C members to establish a separate consortium to develop the roadmap that will guide development across the emerging industry and identify the necessary manufacturing technologies and capabilities. This new consortium will include QED-C members and non-QED-C members across the stakeholder spectrum.

5:00pm **QS-MoA-11 Cryogenic Properties of Discrete Electronic Components for Use in Quantum Measurement Circuits**, *Nikki Ebadollahi*, National Institute of Standards and Technology (NIST)/ University of Maryland, College Park; *P. Shrestha*, National Institute of Standards and Technology (NIST); *D. Krymski*, University of Maryland, College Park; *Y. Hong*, *E. Rissanen*, *J. Pomeroy*, National Institute of Standards and Technology (NIST)

The changes in transistors, capacitors and resistors when they are cooled to cryogenic temperatures are measured to enable the design and fabrication of quantum control and readout circuits. Quantum devices, and eventual quantum computers, function at cryogenic temperatures, and achieving high efficiency requires that the classical and quantum components are positioned closely together within a circuit. Before discrete classical components can be integrated into basic auxiliary circuits for a quantum system, it is essential to understand the properties of these components at 4 K. While the cold temperatures yielded predictable changes for resistor properties, capacitors and transistors underwent significant and unpredictable changes. For the capacitors, the changes in capacitance were largely dependent on the material, dielectric constant, and surface area. The dielectric constant decreases as cryogenic temperatures are reached for some materials. For some capacitors, the capacitances decreased by a factor of 20 in response to the temperature drop. For the transistors, the threshold voltage, transconductance, and transfer curves all notably changed from room temperature to 4 K. Both the threshold voltage as well as the slope of the transfer curve increased significantly at 4 K compared to the behavior at room temperature. Due to the temperature-dependent characteristics of discrete electronic components, circuits must be designed with operating parameters suited for cryogenic temperatures in order to function.

Author Index

Bold page numbers indicate presenter

— B —

Biznarova, J.: QS-MoA-3, **1**

Black, C.: QS-MoA-4, **1**

Bollinger, A.: QS-MoA-4, **1**

Butera, R.: QS-MoA-1, **1**

Bylander, J.: QS-MoA-3, **1**

— E —

Ebadollahi, N.: QS-MoA-11, **2**

— F —

Felbinger, J.: QS-MoA-10, **2**

— H —

Hong, Y.: QS-MoA-11, **2**

— K —

Krymski, D.: QS-MoA-11, **2**

— L —

Li, R.: QS-MoA-4, **1**

Liu, M.: QS-MoA-4, **1**

— M —

McCallum, J.: QS-MoA-8, **2**

— N —

Nanayakkara, T.: QS-MoA-4, **1**

— P —

Poletto, S.: QS-MoA-5, **2**

Pomeroy, J.: QS-MoA-11, **2**

— R —

Rissanen, E.: QS-MoA-11, **2**

— S —

Shrestha, P.: QS-MoA-11, **2**