Thin Films Division
Room 316 - Session TF+EM-MoM

Microelectronics and Spintronics Application
Moderator: John F. Conley, Jr., Oregon State University

8:20am **TF+EM-MoM-1 Rare Earth Thin Oxide Films for Sustainable Energy**, ***Ivona Z. Mitrovic**, H. Finch, S. Almalki, S. Tekin, L. Jones, V. Dhanak,* University of Liverpool, UK*; A. Hannah, R. Valizadeh,* STFC Daresbury Laboratory, UK*; A. Renz, V. Shah, P. Gammon, P. Mawby,* University of Warwick, UK **INVITED**

An ever-greater impetus towards global net zero by 2050 has been driving research in sustainable electronics. This talk will give overview of research led at Liverpool on oxide thin films to be considered as high dielectric constant (high-k) dielectrics on (i) wide band gap (WBG) semiconductor materials for power electronics applications; and in (ii) metal-insulator-metal (MIM) configurations as rectifiers in infrared frequency rectennas for energy harvesting. The WBG semiconductor materials such as GaN and 4H-SiC have emerged as contenders to replace Si in many power electronics applications. High-k oxide materials are necessary for improved electrostatic control over the channel and improved on-current, which in-turn results in higher transconductance for GaN based Metal-Insulator-Semiconductor High Electron Mobility Transistors (MIS-HEMTs). Furthermore, the use of SiO_2 proves to be a bottleneck in exploiting full potential of SiC technology largely due to the unavailability of a reliable high-k dielectric alternative. In this paper, the two rare earth oxide films, Y_2O_3 and Sc_2O_3, prepared by sputtering, have been investigated in terms of their band alignment and interface properties on both GaN and 4H-SiC substrates using variable angle spectroscopic ellipsometry and X-ray photoelectron spectroscopy. Furthermore, this study includes applicability of Sc_2O_3 for use in MIM diodes for rectenna. The comparison to state of the art devices that mainly include Al_2O_3 and HfO_2 films has been discussed with the aim of paving the way forward for rare earth thin oxide film applications in driving sustainable future.

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9:00am **TF+EM-MoM-3 TaN Electrical Barrier for High-k MOS Capacitor**, *R. César,* ***José Diniz**,* University of Campinas - UNICAMP, Brazil*; R. Cotrin, E. Joanni, M. Vidal,* Renato Archer Information Technology Center, Brazil

Tantalum nitride (TaN) thin films were used at the interface between high-k titanium oxide (TiO_2) and the silicon substrate. The TaN films were deposited by RF sputtering and three thicknesses 2, 4 and 6 nm were studied. The structural characterization of the films was performed AFM, SEM and EDS. Using the AFM and SEM technique, it was possible to note that the film is formed by different grain sizes (Annex Fg.1). Using the EDS technique, it was possible to map the chemical elements that make up the TaN film, and it was possible to determine that 93,4% of the TaN film is composed of tantalum and 6,6% is composed of nitrogen.

MOS capacitors were developed using n-type silicon and TiO_2 as the gate dielectric. This oxide was deposited by ALD and has a thickness of 35 nm. Between the oxide and the silicon, TaN was deposited by RF sputering and has a thickness of 2, 4 and 6 nm. These devices have the upper electrode in the square shape and varying its dimension. Tables 1 and 2 in the Annex present the parameters calculated and extracted from the CxV and IxV curves of the MOS capacitors with TaN/TiO_2.

The capacitor with 6 nm of TaN did not present well-defined electrical measurements. This may be due to its thickness which started to act as a resistor between the TiO_2/Si. It can be seen from Tables 1 and 2 (Annex) that, 4 nm of TaN showed higher V_{FB} values than the capacitors with 2 nm of TaN. As seen in the structural characterization of the TaN films, the film has 93.4% tantalum. This metal ion is acting as a potential barrier on the capacitor. The higher the barrier, the higher the voltage must be for the device to work.

The capacitor with 2 nm of TaN showed higher hysteresis values than the 4 nm film, as shown in Tables 1 and 2. The 2 nm and 4 nm TaN capacitors showed $C_{máx}$ in the order of e^{-4} ~ e^{-5} F and e^{-4} ~ e^{-6} F, respectively. The same behavior can be described for $C_{mín}$ values. Both capacitors showed minimum capacitance on the order of e^{-5} ~ e^{-6} F.

Both capacitors presented effective charge density (Qo/q) in the order of e^{17} ~ e^{20} /cm^2. This result confirms that tantalum metal ions from the TaN film are interacting with the silicon substrate. Confirming the changes in the values of V_{FB}, $C_{máx}$ and $C_{mín}$. This indicates that variations in the dipole are occurring at the TiO_2/TaN/Si interface, due to chemical reactions between the two materials. These variations in the dipoles can change the value of the flat band voltage making it positive, which is the case for the two TaN film capacitors.

9:20am **TF+EM-MoM-4 Internal Photoemission (IPE) Spectroscopy Measurement of Interfacial Barrier Heights in Pristine and Poled Ferroelectric Hafnium Zirconium Oxide Devices**, ***Jessica Peterson**,* Oregon State University*; T. Mimura,* Gakushuin University, Japan*; J. Ihlefeld,* University of Virginia*; J. Conley,* Oregon State University

Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) has attracted interest for CMOS memory and logic due to ease of integration as HfO_2 is already widely used. After device preparation, a "waking" process involving repeatedly sweeping a field across the material is necessary to induce ferroelectric behavior.[1] Use of HZO in CMOS applications requires knowledge of interfacial energy barriers in the specific film stacks used. Internal photoemission (IPE) spectroscopy is the only method of measuring barrier heights in working devices. IPE measurements of energy barriers have been reported for as-deposited HZO.[2] Here we investigate how waking and poling impact barriers.

20 nm thick HZO was deposited on a TaN coated Si substrates via atomic layer deposition (ALD) using 102 supercycles of HfO_2 (TDMAH) and ZrO_2 (TDMAZ), then coated with a 20 nm blanket TaN film and annealed at 600°C for 30 seconds. The top TaN layer was then stripped before depositing an optically transparent top electrode of 5 nm TaN / 5 nm Pd. Devices were woken by performing 5000 ±5V cycles. Woken devices were poled by applying a 0 to +4V or 0 to -4V square pulses. IPE measurements were taken by applying a voltage to the bottom electrode while grounding the top electrode. Positive (negative) polarity was used to assess the top (bottom) barrier. At each applied field, $\mathcal{E}_{app}$, photon energy incident on the top electrode was swept from 2 to 5 eV. Extracted spectral thresholds were plotted vs. $\mathcal{E}^{1/2}$ and extrapolated to zero field to account for any Schottky field induced barrier lowering.

For unwoken devices, the top and bottom HZO/TaN barriers were 2.6 and 2.9 eV, respectively, indicating the influence of processing. The waking process caused an increase in the top barrier to 2.9 eV while the bottom barrier was unchanged within error. Positive poling caused a reduction in both top and bottom barrier heights to 1.9 and 2.5 eV, respectively, for positive sweep first. Negative poling caused a reduction in top and bottom barrier heights to 2.1 and 2.2 eV, respectively, for negative sweep first. While field sweep direction did not impact barrier heights on pristine devices, it did have a small impact on poled devices, to be discussed. The lower barrier heights for poled devices and polarity dependence are consistent with a recent report on the impact of cycling on TiN effective work function on HZO, and suggest a role for oxygen vacancy migration.[3] This work provides insight into the impact of waking and poling on barriers in HZO devices, information needed for integration.

[1] Grimley et al., AEM 2, 1600173, (2016).

[2] Jenkins et al., ACS AMI 13, 14634 (2021).

[3] Hamouda et al., APL 120 202902 (2022).

11:00am **TF+EM-MoM-9 On-Chip ALD LiPON Capacitors for High Frequency Application**, *K. Ahuja,* University of Maryland, College Park*; V. Sallaz, F. Voiron,* Murata, France*; P. McCluskey, G. W. Rubloff,* University of Maryland, College Park*;* ***Keith E. Gregorczyk**,* University of Maryland

The increase in demand for miniaturized portable electronics has led to increased use of capacitors for power conditioning applications. In order to increase the efficiency of the electronic circuits, the ICs embedded in these devices require stable DC supply voltage, this requires optimization of power distribution networks (PDN). A common approach consists of placing a decoupling capacitor close to the ICs thus shorting the inductive path that limits the current flowing from the slow and distant battery and thus increasing the efficiency of the system. The traditional aluminum electrolytic capacitors and MLCCs are used for this application but they are limited by high intrinsic parasitic inductance, bulky volume, rigid shapes, and low energy density. Next-generation devices with solid-state electrolyte (SSE) using atomic layer deposition (ALD) provide a few advantages to such applications. (1) Thin, ionically conductive materials allow for significant device dimensions reduction avoiding the above-mentioned problems, (2) easy integration with semiconductor chip manufacturing, and (3) an active community developing new materials regularly.

Here, we demonstrate ALD of ultra-thin film lithium phosphorus oxynitride (LiPON) as an inorganic SSE exhibiting both EDLC and electrostatic behavior. Two polymorphs of ALD LiPON ($Li_{3.47}PO_{3.43}N_{0.24}$ and Li_2PO_2N) are deposited between gold current collectors on silicon wafers. The ionic conductivity of the polymorphs is 6.82× 10^{-8} S/cm and 5.42× 10^{-7} S/cm respectively. The ionic conductivity was determined to be the most important metric effecting the charge storage mechanism. Both the LiPON capacitors exhibit an electric double layer behavior with a capacitance of 15 uF/cm^2 and a low leakage current (<20 nA/cm^2) at 2V. The $Li_{3.47}PO_{3.43}N_{0.24}$ shows EDLC behavior up to 1 kHz at 55°C whereas the Li_2PO_2N shows a similar behavior up to 10 kHz. Beyond this frequency, both the polymorphs show an electrostatic behavior with a high dielectric constant (13).

These results highlight the advantage of ALD LiPON as thin-film SSE for capacitors that shows EDLC behavior to an extended frequency limit (10kHz) for state-of-the-art applications. The electrostatic behavior observed at high frequency (>10 kHz) further expands the application window for high-frequency decoupling applications. The high energy density and on-chip integration allow for easier process control and design flexibility for advanced PDN. Further, utilization of ALD's inherent conformality in 3D nanostructures can extend the reach of these solid-state ionic capacitors to increasing energy density metrics along with on-chip integration.

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11:20am **TF+EM-MoM-10 Designer Heusler Half-Metals for Ultra-Fast Spintronics*, Avik Ghosh,*** University of Virginia **INVITED**

Heusler alloys have several interesting attributes, such as a practical realization of the Slater-Pauling rule for half-metallicity with nearest neighbor interactions. Using Density Functional Theory we scavenged through a large number (1359) of full, half and inverse Heuslers, verified their thermal (heat of formation) and chemical (complex Hull distance) stability, and identified multiple potential Slater-Pauling semiconductors and half-metals (e.g. Fe2MnGe, layered Fe1.5TiSb, Co1.5TiSn). In addition, we found some zero momentum half-metals with negative formation energy, materials that are potentially insensitive to magnetic fields while carrying substantive spin currents. Interestingly, uniaxial anisotropy is seen to be induced in some of the L21 and C1b Heuslers (e.g. NiMnSb, CoTiSn) adjoining MgO without losing their half-metallicity, yielding potential magnetic electrode materials with large ballistic tunnel magnetoresistances. Finally, spin flip scattering rates are calculated with KKR and ballistic currents using quantum kinetics, showing that some of these Heuslers have low spin damping, making them good potential candidates for supporting room temperature, ultra-small Neel skyrmions.

Author Index

Bold page numbers indicate presenter