Plasma Science and Technology Division
Room 305 - Session PS1+TF-TuA

Plasma Processing for Advanced Emerging Memory Technologies, Advanced Packaging and Heterogeneous Integration

Moderators: Hisataka Hayashi, KIOXIA, Japan, **Samson Odunuga**, Intel Corporation

2:20pm **PS1+TF-TuA-1 Study of Residues Formation after Ge-Rich GST Etching Using Halogen Gases**, ***Benjamin Fontaine***, STMicroelectronics, France; *C. Boixaderas,* Univ. Grenoble Alpes, CEA, Leti, France; *J. Dubois, P. Gouraud, A. Rival,* STMicroelectronics, France; *N. Posseme,* Univ. Grenoble Alpes, CEA, Leti, France

Non-volatile memories patterning is being more and more challenging with dimension reduction. Germanium-antimony-tellurium alloy (GST) has been well studied for phase-change random access memory (PCRAM) applications. Previous publications have proven the interest of using halogen plasmas to etch GST with etch rate range between 200 $nm.min^{-1}$ and 700 $nm.min^{-1}$ using HBr, CF_4 or Cl_2 chemistries. The etching results in halogen implantation in the first nanometers of the material with less modified surface and better roughness using the HBr chemistry. Despite these improvements, complementary analyses recently revealed a defectivity increase (residue formation) after etching and air exposure.

In this work, we propose to study the evolution of the surface state from the first hours of air exposure to several days after the etching using Ge-rich GST full-sheets. We compared the halogen chemistries showing residues formation in the first moments of air exposure after the etching step. Throughout a kinetic study, we showed the criticality of brief air exposures and found the optimal time required for the material protection.We observed a high level of defectivity after 24h of air exposure.

Residues are known for altering devices operation. XPS and EDS analyses revealed that important surface oxidation is present when residues appear. Complementary analyzes revealed that moisture environment has also a catalytic effect on the residue formation. Based on these results, a detailed mechanism responsible of residues formation will be presented.

Using this mechanism, in-situ Post-Etching Treatments (PETs) will be proposed in order to prevent residues formation. We will implement the best PETs on real devices to verify their effectiveness.

2:40pm **PS1+TF-TuA-2 Magnetron Plasma Sputtered $Ge_2Sb_2Se_4Te$ as a Non-Volatile Optical Switch Material**, ***Steven Vitale***, *P. Miller, P. Robinson, C. Roberts, V. Liberman,* MIT Lincoln Laboratory; *Q. Du, Y. Zhang, C. Popescu, M. Shalaginov, T. Gu,* Massachusetts Institute of Technology; *M. Kang, K. Richardson,* University of Central Florida; *C. Rios,* University of Maryland; *J. Hu,* Massachusetts Institute of Technology

Commercial technologies such as non-volatile memory, integrated photonic circuits, and compact optics are enabled by amorphous-to-crystalline transition of phase change materials (PCMs); for optical applications, the key feature of PCMs is the ability to change the optical properties (n, k) of the material by switching between a high-index crystalline phase and a low index amorphous phase. Here, we study the phase transition of an IR-transparent PCM, $Ge_2Sb_2Se_4Te$ (GSST), deposited using an AJA combinatorial magnetron plasma sputtering system. The film composition was tuned by varying the RF power to each of the Ge, Sb, Te, and $GeSe_2$ sputtering targets based on measurements from an in-situ EDX spectrometer.

Microheaters were fabricated in a fully-depleted silicon-on-insulator technology and coated with GSST. Microheater temperatures in excess of the melting point of GSST (900 K) were achieved. The small mass of the microheater allows for a quenching rate in excess of 10^7 K/s which is critical for amorphization as slower cooling causes recrystallization. The microheater chips were mounted in a Raman microscope and connected to pulsed electronics and the GSST structures was measured after amorphization or recrystallization heater pulses. The characteristic Raman peak of amorphous GSST occurs at 157 cm^{-1} and is consistent with Ge-4Se tetrahedral units. The characteristic Raman peak of crystalline GSST occurs at 120 cm^{-1} and is consistent with Ge-6Se octahedral units. The fundamental crystalline-to-amorphous transition appears to be reduction in Ge coordination from six to four, with the excess selenium atoms forming an amorphous Se-Se network. The amorphous-to-crystalline transition requires breaking the Se-Se network and increasing the Ge coordination from four to six. The measured activation energy for this transition is very close to the Se-Se bond energy and is thus consistent with the proposed mechanism. Enabled by the microsecond heater response we measured an ultrafast time-temperature-transformation diagram for GSST.

No irreversible chemical change (such as oxidation or decomposition) was observed up to 1000 crystallization-amorphization cycles. Lumerical simulations of a telecom-relevant silicon photonic switch show that the measured variation in octahedral/tetrahedral content allows for acceptable insertion loss variability but improved microheater temperature reproducibility will reduce variation in output port contrast.

3:00pm **PS1+TF-TuA-3 Phase-Change Memory Materials Processing Requirements**, ***Luxherta Buzi***, IBM Research Division, T.J. Watson Research Center; *H. Cheng,* Macronix; *M. Hopstaken,* IBM Research Division, T.J. Watson Research Center; *L. Gignac,* IBM Research, T. J. Watson Research Center; *C. Tabachnick, J. Papalia, H. Miyazoe, S. Engelmann, R. Bruce,* IBM Research Division, T.J. Watson Research Center

Switching of Phase Change Memory (PCM) material between crystalline and amorphous phase with electrical pulses and optical properties make it an important candidate for storage class memory and neuromorphic computing [1-2]. These PCM materials (e.g., GeSbTe and its derivatives) can be damaged during plasma etch processing leading to poor performance and yield [3-4]. Surface oxidation of PCM materials can substantially alter switching properties therefore, in-situ encapsulation has been viewed as a favorable solution [5]. It is imperative that RIE and encapsulation mitigate damage or oxidation of PCM material during integration. This paper reviews the effects of etch chemistry, temperature, plasma reactor, and post RIE processing on material properties [3, 6]. In-situ encapsulation of GST and tuning of plasma parameters, caused controlled SiN film deposition with simultaneous selective etching of GST [6]. We have also demonstrated that using alternative chemistry for PECVD film encapsulation can improve GST switching properties and provide a good barrier for GST oxidation.

[1] H. Tsai, et al., Journal of Physics D: Applied Physics, 51, (2018).

[2] S. Ambrogio, et al., Nature, 558, 60-67 (2018).

[3] L. Buzi, et al., SPIE 2021 doi: 10.1117/12.2581706

[4] H-Y. Cheng et al 2019 J. Phys. D: Appl. Phys. 52 473002

[5] P. Noe et al., Acta Materialia 110 (2016) 142-148

[6] L. Buzi, et al., SPIE 2022, Advanced Etch Technology and Process Integration for Nanopatterning X

3:20pm **PS1+TF-TuA-4 Exploration of Alternative Hard Mask Materials for the IBE Patterning of 50nm Pitch STT-MRAM High Density Orthogonal Pillar Array**, ***Romuald Blanc***, *L. Souriau, W. Devulder, S. Couet, F. Lazzarino,* IMEC, Belgium

In order to approach the bit density of dynamic random access memory (DRAM), spin-transfer torque (STT) magnetic random access memory (MRAM) requires to be scaled down to pitch 50nm and below[1,2]. To fabricate 50nm pitch STT-MRAM high density pillars, ion beam etching (IBE) is used to pattern the magnetic-tunneling junction (MTJ). This etch technique relies mainly on physical ion sputtering which does not allow high selectivity to the hard mask[3], therefore a robust material is needed to avoid excessively thick hard mask and high pillar aspect ratio.

In this talk, we present the etch rate of multiple materials deposited in 300mm production tools etched with different with ion beam etching conditions. Then we demonstrate the patterning of a hybrid hard mask composed of high-density diamond-like carbon (DLC) to increase etch selectivity and TiN which will become the STT-RAM top electrode. Finally, the interest of this hybrid DLC/TiN hard mask is evaluated for the patterning of the MTJ stack with IBE.

References:

[1] Lei Wan et al, *Fabrication and Individual Addressing of STT-MRAM Bit Array With 50 nm Full Pitch*, IEEE TRANSACTIONS ON MAGNETICS, VOL. 58, NO. 5, MAY 2022

[2] Murat Pak et al, *Orthogonal Array Pillar Process Development for High Density 4F2 Memory Cells at 40nm Pitch and Beyond*, SPIE Advanced Lithography 2022, Paper 12051-45

[3] Kuniaki Sugiura et al, *Ion Beam Etching Technology for High-Density Spin Transfer Torque Magnetic Random Access Memory*, Japanese Journal of Applied Physics 48 (2009) 08HD02

4:20pm **PS1+TF-TuA-7 Patterning Approaches for Integration of Complex Metal Alloys Towards Advanced Memory and Compute Applications**, ***Shreya Kundu****, F. Lazzarino,* IMEC, Belgium **INVITED**

Increasing need of data processing from core electronic devices is instrumental in driving the innovation of high-density memories and high-performance computing in the semiconductor industry. To sustain this growth in storage and computing domains, novel material systems are being investigated exhaustively due to their promising intrinsic properties. A key challenge here is their satisfactory patterning to enable assimilation into integrated chips.

Patterning studies of complex alloy systems generally aim at finding a suitable etch chemistry which promises good feature profiles with minimal physical and chemical damage. However, when integrated with diverse electrode materials (for e.g. SiN, TiN), it becomes imperative for the patterning investigation to include an additional criterion i.e., the etching of the novel alloy or the electrode should not have an adverse morphological or structural impact on one another, as it can lead to poor electrical performance. Patterning of two types of complex material systems – chalcogenide-based films (GeSbTe, SiGeAsTe/Se) and InGaZnO (IGZO) – displaying etching attributes on opposite ends of the spectrum are discussed here. Chalcogenides find widespread application in resistive, holographic non-volatile memory, and ovonic threshold switches due to their unique electronic and optical response signatures. Therefore, these materials are often integrated with optically conductive electrodes and heat sinks within an electrical circuit[1]. As chalcogenides produce highly volatile halogen-based by-products[2], prolonged exposure to similar etchants used in conventional electrode patterning schemes can cause severe undercuts leading to feature collapse. On the other hand, IGZO, a potential candidate for high performing thin film transistors[3], can be patterned using a hydrocarbon etchant and remains unimpacted by the chemistries used for etching electrode materials[4]. However, IGZO-based residues along electrode sidewalls are common post-patterning, thereby making the devices prone to current leakage.

In this talk, an overview of challenges encountered in patterning complex materials in varied integration schemes is presented followed by a systematic discussion on etch approaches to circumvent them. The repeatability and scalability of the etching schemes are also discussed.

Acknowledgments- to IMEC's Industrial Affiliation Program, IMEC's Active Memory and TIP integration team.

References

[1]N. A. Bogoslovskiy, *et al*. Semiconductors 46, 559 (2012)

[2]Canvel, *et al*, J. Vac. Sci. Technol. A 37, 031302 (2019)

[3]S. Yamazaki, *et al*. Jpn. J. Appl. Phys. 53, 04ED18 (2014)

[4]Zheng, *et al*,Plasma Sci. Technol. 14, 10, (2012)

5:00pm **PS1+TF-TuA-9 Plasma Etch Challenges and Processing Optimization in Spin Logic Device Fabrication**, ***Yann Canvel****, L. Souriau,* IMEC, Belgium

Presently, microprocessor chips rely on the networking of billions of tiny switches, commonly called transistors. These CMOS-based technologies run logic operations via the electron charge to enable data computing for the function of any digital object. In the development of next-generation logic devices, an alternative solution would be to leverage the electron's spin instead of the electron's charge. This specific electron manipulation paves the way towards the fabrication of spin logic devices which promises high performances and low power consumption.

In this communication, close attention will be dedicated to the unique patterning challenges of such architectures. It mainly consists of creating a magnetic interconnect system to propagate, in a controlled way, the information through the magnetic logic circuit. Ion Beam Etch (IBE) technique is used to shape the magnetic track. The critical point is to control the vertical etch of the Magnetic Tunnel Junction (MTJ) stack at nanometric scale. In this frame, a deep understanding of the plasma-surface interaction is required and will be presented here. As a result, some process optimization will be discussed to mitigate the ion-induced damages. Both soft landing and cyclic IBE approaches will be highlighted as proof of concept.

Raymenants, E. *et al.* Nanoscale domain wall devices with magnetic tunnel junction read and write. *Nat Electron***4**, 392–398 (2021).

Raymenants, E. *et al.* All-Electrical Control of Scaled Spin Logic Devices Based on Domain Wall Motion. *IEEE Trans. Electron Devices***68**, 2116–2122 (2021).

Raymenants, E. *et al.* Magnetic domain walls: from physics to devices. in *2021 IEEE International Electron Devices Meeting (IEDM)* 32.3.1-32.3.4 (IEEE, 2021).

5:20pm **PS1+TF-TuA-10 Effects of Bias Frequency on High Aspect Ratio Etching Using Voltage Waveform Tailoring**, ***Florian Krüger****,* University of Michigan*; H. Lee, S. Nam,* Mechatronics Research, Samsung Electronics Co., Ltd., Republic of Korea*; M. Kushner,* University of Michigan

The continuing reduction of feature sizes and increasingly high aspect ratios (HAR) in plasma etching pose major challenges to high volume manufacturing of nanoscale semiconductor devices. Capacitively coupled plasmas (CCPs) are an important tool for HAR etch processes. In these systems, the DC self-bias is used as a measure of mean ion energies incident onto the wafer. DC bias is coupled to the asymmetry of the system which can be a function of geometry, material differences, magnetic configurations and the use of non-sinusoidal voltage waveform tailoring (VWT) through the electrical asymmetry effect.

We computationally investigated the consequences of bias frequency on ion energy distributions (IEDs) and SiO_2 etch properties when varying the electrical asymmetry of the bias waveform.The electrical asymmetry is controlled with the phase shift of the even harmonics ϕ of a multifrequency waveform.The system is a CCP with high frequency source power and low frequency bias power.The plasma was sustained in fluorocarbon gas mixtures at 40 mTorr. The bias waveform consisted of 5 harmonics with a base frequency of 1 to 10 MHz. The gas phase simulations were performed using the Hybrid Plasma Equipment Model (HPEM).Using reactive fluxes to the wafer from the HPEM, etching of a HAR via in SiO_2 was simulated using the Monte Carlo Feature Profile Model.The resulting features were evaluated based on etch rate, etch depth and distortion.

We found that at sufficiently high bias frequencies where ions are unable to react to time-varying fields in the sheath, IEDs are dominantly affected by time-averaged sheath electric fields. Mean ion energy is correlated to the DC self-bias, which in turn is correlated to ϕ**.** In this regime maximumion energies occur when ϕ=0, and electrical asymmetry as well as DC self-bias magnitude are maximum. The resulting etch features have most desirable qualities when ion energies are high at low phase angle.

This trend does not apply and, in fact, reverses for low bias frequencies where ions are able to dynamically react to transient electric fields. This leads to temporal variations in ion energies and fluxes which result in higher ion energies at higher phase angles and lower electrical asymmetry. The trend of reversal in ion energies with phase angle also translates to the etch feature having better overall quality at high phase angle. We conclude that when using VWT techniques for process control in etch systems, there are two frequency regimes (dynamic-ions and stationary-ions) having different control mechanisms.

Work supported by Samsung Electronics and the National Science Foundation.

5:40pm **PS1+TF-TuA-11 Wafer Bevel Deposition by Localized SiO_2 and Si_3N_4 PECVD and Application to 3D Integration**, ***Francois Boulard****, F. Fournel, V. Lapras, L. Brunet, D. Truffier-Boutry,* CEA-University Grenoble Alps, France*; P. Ruault,* Lam Research, France*; M. Keovisai,* Lam Research*; C. Porzier, V. Gros, N. Posseme,* CEA-University Grenoble Alps, France

As 3D integration schemes move forward new process challenges arise. One of them is to manage contamination issues of multiples stacked wafers. Particularly, wafers edge and bevel are known to be the source of delamination or defects, as metals or particles contaminations[1-3]. This is even more critical after bonding when back-end of line wafers are reprocessed on front-end tools[4]. In this paper, we present a strategy consisting in encapsulating the bevel area in a single process step. SiO_2 and Si_3N_4 are deposited by PECVD at 350°C on blanket 300mm Si and CMOS + 4 BEOL levels wafers. We study the influence of pressure, RF power, and single or dual frequency plasma excitation on deposition rate, refractive indexes, and films stoichiometries by XPS. No deposition occurs on most of the top surface since the gap between the wafer front side and the top grounded electrode remains below 1 mm. On the wafer edge and bevel, where plasma and deposition take place, films wet etch rates confirm oxide and nitride excellent qualities. The radial deposition profiles is characterized by ellipsometry and scanning electron microscopy cross section. The integration of bevel deposition on CMOS+M4 products is studied. We demonstrate the compatibility of the approach with top tier

bonding and the effectiveness of the encapsulation to control BEOL metal contamination.

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(2)A.Vert, et.al., 2015 26th Annual SEMI Advanced Semiconductor Manufacturing Conference, ASMC 2015, 7164420, pp. 362-366

(3)M.C. Silvestre, et.al., 2016 27th Annual SEMI Advanced Semiconductor Manufacturing Conference, ASMC 2016, 7491136, pp. 124-128

(4)L. Brunet, et. al., Technical Digest - International Electron Devices Meeting, IEDM [https://www.scopus.com/sourceid/26142?origin=resultslist], 2018-December,8614653, pp. 7.2.1-7.2.4

6:00pm **PS1+TF-TuA-12 Plasma Etching of Copper for the Microfabrication of High-Density Interconnects in Advanced Packaging**, ***Juliano Borges***, *M. Darnon, Y. Beilliard, D. Drouin,* Université de Sherbrooke, Canada

Low-cost and high-density redistribution layers (RDL) in integrated circuits packaging are essential to support further development in the fields of high-performance computing and internet of things. Indeed, both require low-cost electronic systems capable of delivering higher bandwidths, improved operation speeds, and enhanced power performance, which can be done by in-package multi-chiplets interconnection.

Organic or silicon interposers have been developed to allow the connection of dies in 2D configurations. Even if silicon-based interposers offer the best interconnects density, they cannot be used in high-frequency applications due to the high resistive losses induced by silicon and their cost is prohibitive for consumer electronics applications. High-density RDL fabrication on organic interposers is therefore required for high-frequency operation and low-cost manufacturing. However, conventional organic interposer fabrication methods by semi-additive processes are not compatible with high-density RDL (<2 µm pitch) because of isotropic wet etching of the seed layer. On the other hand, damascene processes cannot be performed on organic substrates because of substrate warpage. We propose to revisit copper etching processes for high-density RDL fabrication on organic substrates.

Chlorine-based plasmas have been explored as an alternative for etching copper, generally employing cyclic approaches. $CuCl_2$ species are formed upon exposure to Cl radicals and can be transformed into volatile Cu_3Cl_3 when exposed to hydrogen [1]. We developed a one-step $Ar/Cl_2/H_2$-based plasma in an inductively coupled plasma (ICP) chamber with a cathode temperature of 200°C. Using this process, we demonstrated the anisotropic plasma etching of copper with an etch rate of 500 nm/min. A specific seasoning and cleaning process was also set up to provide reproducible etching conditions with no significant chamber contamination after cleaning. By optimizing the etch process, we were able to fabricate high-density copper-based RDL with a pitch of 2 µm. Preliminary tests validated the compatibility of the process with organic substrates.

These results demonstrate the capability of plasma etching processes to etch copper for the fabrication of high-density RDL on an organic substrate for advanced packaging applications.

[1]N. S. Kulkarni and R. T. DeHoff, “Application of Volatility Diagrams for Low Temperature, Dry Etching, and Planarization of Copper,” J. Electrochem. Soc., vol. 149, no. 11, p. G620, Oct. 2002, doi: 10.1149/1.1513986.

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