Plasma Science and Technology Division
Room 315 - Session PS-ThM

Plasma Processing for Advanced Semiconductor Devices

Moderators: John Arnold, IBM Research Division, Albany, NY, **Kenji Maeda**, Hitachi High Technologies America Inc.

8:00am **PS-ThM-1 Dry Etch Solution to a Challenge in Si/SiGe Dual Channel Process Integration**, ***Yohei Ishii***[1], Hitachi High-Tech America, Inc.; *R. Sugano,* Hitachi, Ltd., Japan; *Y. Lee, W. Wu,* Taiwan Semiconductor Research Institute, Taiwan; *L. Kovatch,* Hitachi High-Tech America, Inc.; *K. Maeda, M. Miura,* Hitachi High-Tech Corporation, Japan **INVITED**

Continuous improvement in terms of device scaling has been made in order to follow Moore's law. Transition from planar structure into Fin-type Field Effect transistor (FinFET) was incorporated so as to obtain higher drive current and lower leakage. To further enhance the electrical properties, introduction of high mobility channel material in P-FET [1], silicon germanium (SiGe), was utilized, while maintaining silicon (Si) in N-FET. This brought up new challenges that are related to not only etch controllability between silicon and silicon germanium, but also interface quality on SiGe channel.

In this presentation, we will discuss the etching challenge in the dual channel fin application. In the fabrication scheme, Si and SiGe need to be etched simultaneously, which requires etched rate controllability between the two materials. However, SiGe etch rate is higher than Si under halogen chemistries. In this investigation, we developed a novel plasma process that controls the etching characteristics (i.e., higher Si etch rate than SiGe) [2], leading to Si-SiGe etched amount control. We will reveal the etch mechanism of the plasma process utilizing surface analysis and ab-initio calculation.

In addition to the etch control, interface condition between gate oxide and SiGe channel is also critical. Sub-threshold can be improved by reducing interface trap density at the interface [3], which can be achieved by obtaining a Si-rich surface. There are a few conventional methods that can achieve a Si-rich surface on SiGe such as atomic layer deposition of Si cap over SiGe [4] and GeOx scavenging [5]. All of these require high temperature processes that cause issues such as atomic diffusion and strain relaxation. In this investigation, we will introduce a plasma treatment at room temperature that creates Si-rich surface. We investigated the mechanism of the surface modification into a Si-rich surface on SiGe under the plasma treatment [6]. We will also present how this has an impact on reducing interface trap density in terms of electrical performance.

[1]. O. Weber et. al., IEDM Tech. Dig., p.719, 2007

[2]. Y. Ishii et. al., Jpn. J. Appl. Phys. **57**, 06JC04 (2018)

[3]. C. H. Lee et. al., IEDM Tech. Dig., p.31.1.1., 2016

[4]. H. Mertens, et al., VLSI Tech. Dig., p.58, 2014

[5]. C.H. Lee, et. al., VLSI Tech. Dig., p. 36, 2016

[6]. Y. Ishii, et. al., IEEE J. Electron Devices Soc. **7**, 1277 (2019)

8:40am **PS-ThM-3 Investigation into the Effect of Plasma-Deposited $SiCl_4/O_2$ Chamber Wall Coatings on the Selective Fluorine-Based Etching of TaN with Respect to Polycrystalline Silicon and Silicon Oxide**, ***Ivo Otto IV***, Tokyo Electron Ltd.; *C. Vallée,* SUNY Polytechnic Institute; *K. Yu, S. Kal, A. Mosden, P. Biolsi,* Tokyo Electron Ltd.

Tantalum nitride (TaN) is widely used as a crucial component of diffusion barriers within the back-end-of-the-line (BEOL) because of its strong dielectric adhesion and ability to scale low in-plane resistivity and diffusion-blocking capability to sub-5 nm thicknesses. In order to create the BEOL interconnect superstructure, a cyclical process of conductor and liner deposition and etching, followed by dielectric capping must be completed. In this paper, we will explore the use of inductively-coupled plasma (ICP) discharges containing NF_3/Ar, NF_3/O_2/Ar, and $NF_3/SiCl_4$/Ar mixtures for the isotropic, dry etching of TaN; relying on radically-based etch, without non-selective ion bombardment. The aforementioned radically-based process is sensitive to chamber wall condition during the etching process; therefore, we considered that such methods often employ wall coatings in order to achieve superior etch uniformity and wafer-to-wafer reproducibility. This process is outlined in Figure 1; comparing the process utilizing coating and without utilizing coating. PATH A includes chamber conditioning without coating followed by the etching of the sample wafer, while PATH B includes the application of coating prior to sample wafer processing. The mechanism of $SiCl_4$ and O_2 PECVD of SiO_2 has been extensively studied, while the impact of the coating itself on metal and metal nitride etching has not been so well explored. The aforementioned dry-etching chemistries for the removal of TaN are compared with and without using a $SiCl_4/O_2$ chamber coating: comparing the etching process of the TaN film and etch selectivity to polycrystalline silicon and silicon dioxide. In-situ optical emission spectroscopy is utilized to find that the $SiCl_4/O_2$ chamber coating reacts with the ICP discharge to modify relative species densities when compared to a discharge without the chamber coating applied. Furthermore, modification does not only occur within the discharge, but at the film surface, where we use spectroscopic ellipsometry (SE) to find the etching selectivity of the TaN film is significantly changed with respect to the polycrystalline silicon and silicon oxide upon coating application. O_2 and $SiCl_4$ are separately added directly to the plasma discharge in order to characterize the effect of coating constituent gases and to ascertain if a similar affect to coating addition could be attained with direct addition of O_2 or $SiCl_4$ to the discharge. X-ray photoelectron ellipsometry is utilized in order corroborate SE findings, but to also give an idea of the fluorine-based etching pathway the TaN undergoes towards achieving full removal.

9:00am **PS-ThM-4 Influence of Aspect Ratio on Isotropic Etch Process: A Case Study with SiCN Material**, *P. Luan,* ***Andrew Nolan***, *Y. Yoshida, Y. Han, P. Biolsi,* TEL Technology Center, America, LLC, USA; *K. Ken, N. Ikezawa,* Tokyo Electron Ltd., Japan

Etching of trenches and holes into low-k dielectrics is an indispensable process in very-large-scale integration (VLSI) applications. As the critical dimension (CD) size shrinks aggressively with the advancement of technology nodes, the same etch amount (EA) leads to significantly increased aspect ratio (AR, calculated by EA/CD). In this work, we use SiCN as an exemplary low-k dielectric to investigate the effect of AR in isotropic etch processes where F-containing neutrals are the dominant etchant and the effects from ions are minimized. Blanket SiCN films and Si shadow mask were used to form a testing structure with which AR ranging from 0:1 to 70:1 can be evaluated. The etch amount of SiCN materials and their refractive index were evaluated using Spectroscopic ellipsometry (SE). The surface composition pre- and post-etch processes were examined by X-ray photoelectron spectroscopy (XPS), and Fourier transform infrared spectroscopy (FTIR) at various ARs. We found that the etch rate and surface composition inside the shadow mask are dramatically different from those outside, which reflects the effect of ions on SiCN etching. With higher AR, the etch rate of SiCN reduces whereas the surface composition of the etched SiCN film shows the formation of F-containing etch byproduct concentrated in the AR range between 15:1 and 45:1. The etch byproduct shows a characteristic XPS N1s peak at 403.8 eV, a Si2p peak at 105.1 eV, and a large amount of Fluorine. The accumulation such byproduct in this particular AR range could be resulted from the transport property of neutral-reactants from plasma and the lack of ion bombardment.

11:00am **PS-ThM-10 Plasma Etch Fundamentals and Engineering: Advancing Interconnect Scaling**, ***Theo Standaert***, IBM Research Division, Albany, NY **INVITED**

Since IBM introduced Cu in 1997, the scaling of these interconnects has been relentless for more than two decades. Hundreds of miles of wiring are now deployed in a mindboggling small footprint for the most advanced computer chips, completing the electronic network for billions of transistors. Plasma etch has been and continues to be one of the essential process steps responsible for interconnect scaling. This review starts with some personal experiences as a young engineer, shortly after graduating in the field of plasma etch and surface science. Science and engineering are very different domains. Both are key for advancing and developing new technologies. In case of plasma etch engineering, one must understand the other processes and their constraints, both up- and down-stream in the manufacturing flow. Problems or challenges are rarely confined to a single process or sector. An example of isolated via etch-stop in a low-k dielectric will illustrate how very different engineering can be from science, and an interesting outlook for students and future engineers who are primarily focusing on science now. The review then continues through the past two decades, highlighting some of the key engineering innovations together with the plasma etch processes that enabled them, including patterning solutions for EUV and multi-layer. Finally, there are the future opportunities of interconnect scaling, arguably even more exciting than the past!

[1] **2020 PSTD Young Investigator Award Winner**

11:40am **PS-ThM-12 Exploring the Use of Tungsten-Based Hard Masks in Beol Interconnects for 3 nm Node and Beyond**, ***Daniel Montero***, *V. Vega-Gonzalez, H. Puliyalil,* IMEC, Belgium*; J. Nie, J. Yang,* LAM Research*; F. Schleicher,* IMEC, Belgium*; K. Mclaughlin,* LAM Research*; J. Versluijs, F. Lazzarino, S. Park, Z. Tokei,* IMEC, Belgium

Scaling down the average chip size is one of the main drivers in the microelectronics industry, as it broadens the range of applications when smaller, cheaper, more efficient and more powerful chipsets can be installed in tighter packaging. However, scaling down does come with a price, the increased complexity during design and processing. An improvement from the stack composition point of view (materials and thicknesses) is needed, to keep up with the increasing demands while chip downscaling. Novel chip technology nodes require thinner patterning layers, to enable more advanced lithography steps (e.g., EUV lithography), which requires thinner photoresist layers, and therefore, thinner stacks, to transfer the pattern to the dielectric layers underneath [1]. It is in this context when robust and hard to etch materials (Hard Mask materials, HM), with higher etch selectivity are needed.

In the Back End Of Line (BEOL), TiN has been used as the HM of choice from many years in dual damascene applications [2]. As we approach to iN3 nodes and beyond, we face several issues while downscaling. The selectivity during dielectric etch may not be high enough to adequately transfer the pattern (line breaks, increased line roughness, loss of self-alignment during via patterning). TiN layer stress may not be suitable for tighter pitches, which may end up causing line wiggling. Another aspect is that fluorine-based chemistries, used to pattern the dielectrics below the HM, may form TiF salts, eventually leading to possible fail mechanisms.

Tungsten-containing layers have been proposed as viable candidates to replace TiN as HM in more advanced nodes. In this abstract, we first screen different W-containing layers deposited on blanket wafers, with varying W percentage content. Then, we demonstrate the etch development process of three different W-containing layers, acting as HM in line space patterning at tight pitches: at Metal Pitch 36 nm (MP36, line CD 18 nm), by means of an EUV single print lithography process, and at MP21 (line CD 10.5 nm), realized by means of ArFi lithography process and using a self-aligned quadruple patterning (SAQP) exercise. A first trench etch patterning exercise is done on SAQP P21 line space patterns to extract the average line roughness and HM selectivity values.

References

[1] D. de Simone et al, High-NA EUVL: the next major step in lithography. https://www.imec-int.com/en/articles/high-na-euvl-next-major-step-lithography

[2] H. Shi et al. Plasma processing of low-k dielectrics, chapter 3, ISBN 0470662549

12:00pm **PS-ThM-13 Reactive Ion Etch of Subtractive Metal for Advanced Interconnect**, ***Lijuan Zou***, *Y. Mignot, C. Penny, J. Arnold,* IBM Research Division, Albany, NY*; G. Stojakovic, P. Friddle, S. Schmitz,* Lam Research Corporation

The ability to etch metals in a controlled manner has potential applications at the forefront of advanced interconnect for semiconductor scaling. In this study, the authors evaluate Ru patterning and investigate in depth Reactive Ion Etching (RIE) mechanisms of Ru film in O2/Cl2/CH4 plasma. The etch rate; profile control and mask selectivity of Ru are examined as a function of Cl2/O2 gas ratio; passivation gas CH4 addition and bias power applied. By tuning polymerization, the authors achieve 90º Ru sidewall angle. The impact of various plasma parameters on structural and electrical performance are evaluated using a 300mm Transformer Coupled Plasma (TCP) RIE chamber. The plasma-material interaction is also studied with respect to masking materials. Each of these conditions are evaluated at aggressive critical dimensions to determine the impact of reduced feature size on the ability to anisotropically etch metal structures.

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