Supplemental Information:

Interfaces between III-V semiconductors and high-k dielectrics: Opposite requirements for MOSFET, ferroelectrics, and resistive RAM applications

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Publications on III-V MOSFET interfaces:

[1] R. Timm et al., APL 97, 132904 (2010), doi:10.1063/1.3495776; APL 99, 2229070, doi:10.1063/1.3664399
[2] J. Wu, L.-E. Wernersson, et al., Nano Lett. 16, 2418 (2016), doi: 10.1021/acs.nanolett.5b05253
[3] A. Troian et al., AIP Advances 8, 125227 (2018), doi: 10.1063/1.5054292

Publications on ALD self-cleaning:

[4] R. Timm et al., Nature Commun. 9, 1412 (2018), doi: 10.1038/s41467-018-03855-z
[5] G. D'Acunto et al., ACS Appl. Electron. Mat. 2, 3915 (2020), doi: 10.1021/acsaelm.0c00775

Publications on RRAM interfaces:

[6] Z. Yong, K-M. Persson, et al., Appl. Surf. Sci. 551, 149386 (2021), doi: 10.1016/j.apsusc.2021.149386
[7] M. S. Ram et al., *submitted* (2021)

Publications on ferroelectric HZO interfaces:

[8] A. Persson et al., Appl. Phys. Lett. 116, 062902 (2020), doi: 10.1063/1.5141403
[9] R. Athle et al., ACS Appl. Mat. Int. 13, 11089 (2021), doi: 10.1021/acsami.1c01734

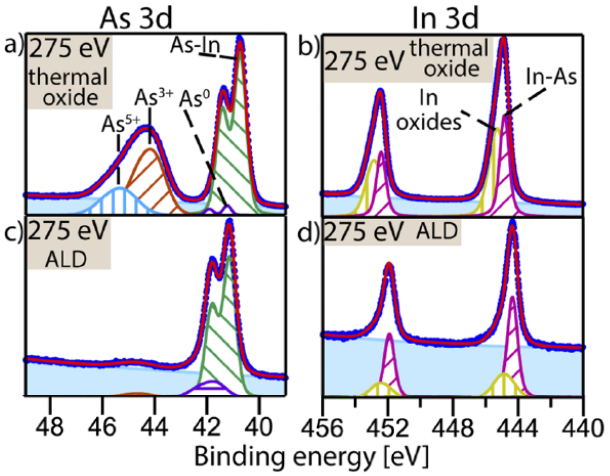

Figure 1: InAs/Al2O3 MOSFET interface studied by XPS [3]

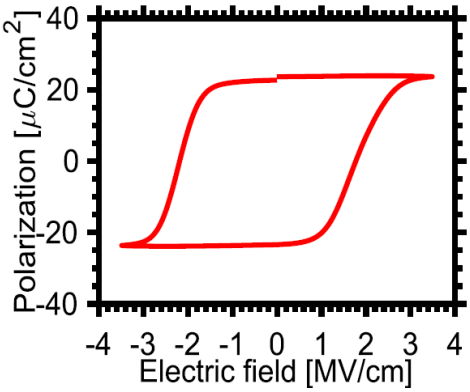

Figure 2: Hysteresis curve at 3.5 V of a 10 nm thin HZO film on InAs [9]

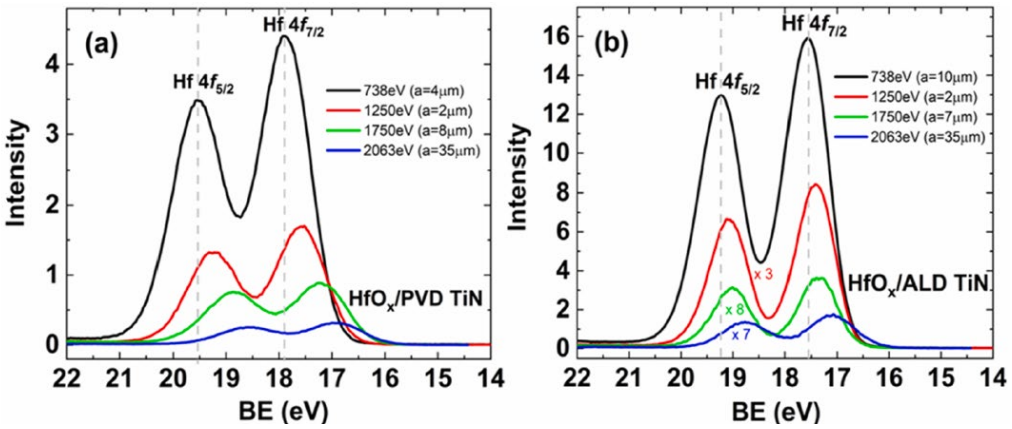

Figure 3: Interface between RRAM HfO_2 and TiN top electrode, for differently deposited metal layers. The XPS Hf core-levels show different amount of interface band-bending. [6]