Electronic Materials and Photonics Division
Room 101A - Session EM+MP+PS-MoM
IoT Session: CMOS, Beyond the Roadmap and Over the Cliff

Moderators: Sean King, Intel Corporation, Wilman Tsai, TSMC

8:20am **EM+MP+PS-MoM-1 Aluminum Gettering Gate for Improving Defect Density in SiGe MOSCAP Devices***, **Emily Thomson**, M Kavrik, A Kummel,* University of California at San Diego

The use of SiGe alloys in place of silicon in semiconductor devices has been anticipated for many years due to its high carrier mobility and tunability of the band gap by varying Ge content. However, widespread use of SiGe in industry has been prevented by the presence of interface defects between the SiGe and oxide layer in MOSCAP devices. It has been shown that Ge-Ox bonds at the interface are the main source of these defects so by encouraging SiOx bonds or discouraging GeOx bonds, interface defects can be minimized. The higher heat of formation of SiOx compared with GeOx allows for the selective destruction of GeOx bonds using an oxygen scavenging metal as the gate metal, causing oxygen from GeOx bonds to diffuse through the oxide layer. Here, aluminum was used as an oxygen scavenging gate in order to achieve a low defect density of 3E11 $eV^{-1}cm^{-2}$. The high-k dielectric HfO_2 was deposited using atomic layer deposition with precursors TDMAH (tetrakis (dimethylamido) hafnium) and H2O and the aluminum gates were deposited using thermal evaporation. MOSCAP devices with nickel gates were fabricated and measured in parallel to show contrast with a non-scavenging gate metal. C-V measurements were used to characterize interface defect density. TEM images confirmed oxygen scavenging by showing a silicon rich SiGe-oxide interface and an Al2O3 layer at the HfO2-Al gate interface.

8:40am **EM+MP+PS-MoM-2 Direct Growth of Single Crystal Compound Semiconductor Materials on Diverse Substrates for Beyond the Roadmap Multifunctional Integrated Circuits***, **Debarghya Sarkar**, R Kapadia,* University of Southern California

Technological advancement in semiconductor devices for the past several decades has been mainly driven by scaling device dimensions to achieve high computational density and thus operational bandwidth. The next generation of technological advancement is likely to come from vertical fine-grain integration of multiple materials for 3D multifunctional integrated circuits. Epitaxial lift-off and transfer processes are currently employed towards realizing such structures, which though successful, have several shortcomings. On the other hand, direct growth of technologically relevant materials on amorphous dielectrics using state-of-the-art vapor-phase crystal growth techniques results in polycrystalline films with uncontrolled morphology unsuitable for high performance devices. As a potential solution addressing these issues, here we report the recent advances made in the templated liquid phase (TLP) growth technique that enables growth of large-area single crystals of compound semiconductors directly on diverse non-epitaxial substrates. We demonstrate growth of optoelectronic materials such as binary III-V InP and InAs, and optical bandgap tuning with ternary III-V materials like InGaP. We also show phase-controlled growth of binary IV-V materials such as Sn_4P_3 and SnP for high capacity anode materials in Li and Na ion batteries. Further, as the first step towards directly integrating multiple materials on the same substrate, we demonstrate atomically-sharp lateral heterojunctions of cubic InP and rhombohedral Sn_4P_3 crystals. We grow these materials in selective area with deterministic template geometry and conformal to underlying device nanostructures on any thermally stable crystalline (Gd_2O_3), amorphous (SiO_2, Si_3N_{-4}, TiO_2, and $Al_{-2}O_3$), or 2D (graphene) substrate. Despite grown on non-epitaxial substrates, the materials have been characterized to have high quality crystallinity, with high optoelectronic quantum yield irrespective of the substrate, and high carrier mobility. These demonstrations potentially mark the beginning of a new genre of material growth technique with increased opportunity for electronic, photonic, optoelectronic and energy devices, and system design with novel functionalities.

9:00am **EM+MP+PS-MoM-3 Going Beyond Traditional CMOS***, **Inge Asselberghs**, I Radu,* IMEC, Belgium **INVITED**

Continuous connectivity, we take it for granted in our daily life, but it did not exist a decade ago. Consequently, the information infrastructure keeps growing and the traditional scaling approach of the transistors could meet with these high demands. Transistor scaling was achieved by increasing performance with a comparable energy consumption while keeping the cost low. However, the traditional scaling approach may run into fundamental physical limits of device switching. Common materials such as Si and SiGe are reaching their materials scaling limit. Therefore, there is a strong drive to explore alternative materials for device scaling. Looking beyond the common charge based devices, there is a full field in exploratory device concepts that rely on spin, exciton or plasmonic states.

From this perspective, we cover several approaches in the search for higher performance and/or lower energy consumption. We firstly review activities on 2D semiconductors for MOSFET application. A large variety of reports on layered materials were published in literature in the last decade, starting with graphene, moving to transition dichalcogenides (MX2) and diving into the properties of materials such as black phosphorus. We will summarize some of this work, and focus on the more stable MX2 variants as an experimental study format. Here we will also describe some device considerations with respect to channel scaling and the role of double gate (2D equivalent of gate-all-around) aspects. Devices with steep-slope concepts are considered potential alternatives to power scaling as it is expected that the supply voltage could be reduced. In this context, we will describe work on tunnel FETs and summarize briefly the so-called negative capacitance devices.

Rather than looking at device scaling only, we will also describe how functional scaling can create an advantage by improving circuits. From this perspective, spintronic majority gates are ideal candidates as it expected a fewer number of devices is required for complex arithmetic circuits. Some majority gates hold the promise of ultra- low energy operation.

9:40am **EM+MP+PS-MoM-5 Suppression of Electronic Defects at HfO_2-SiGe Interface with Selective Surface Oxidation Using Ozone***, **Mahmut Sami Kavrik**,* University of California at San Diego*; V Hou,* TSMC, Taiwan, Republic of China*; E Thomson,* University of California at San Diego*; K Tang,* Stanford University*; Y Taur,* University of California at San Diego*; P McIntyre,* Stanford University*; A Kummel,* University of California at San Diego

Silicon germanium (SiGe) with high-k dielectric is appealing for low power electronics due to high intrinsic carrier mobility of SiGe. However, the SiGe channel in CMOS transistors can be implemented commercially only if low defect SiGe/high-k interface can be fabricated. Studies have shown that electronic defects are mainly generated by interfacial germanium oxide (GeO_x) which can be removed by selective oxygen gettering from GeO_x or selectively forming interfacial silicon oxide (SiO_x).

In this work, selective interface oxidation with ozone is studied. It is shown that ozone pulsing during the oxide ALD process can significantly lower the interface defect density (D_{it}) when the ozone is pulsed after deposition of at least a few monolayers of gate oxide. When ozone pulses are dispersed across the HfO_2 during ALD growth, the electronic defect density is reduced more than 60% compared to control HfO_2 samples. After careful optimization of ozone pulse and forming gas annealing, low interface defect density of $D_{it}=5x10^{11}$ $eV^{-1}cm^2$ with 1.75uF/cm^2 accumulation capacitance was demonstrated for the $HfO_2/Si_{0.7}Ge_{0.3}$ interface. Gate oxide and the interface composition was investigated with STEM-EELS and Si riched composition was observed consistent with DFT models. Suppression of electronic defects at the HfO_2- $Si_{0.7}Ge_{0.3}$(001) interface with SiO_x selective interface oxidation using ozone was demonstrated.

10:00am **EM+MP+PS-MoM-6 Surface Free Energy and Interfacial Strain in HfO2 and HZO Ferroelectric Formation***, **Andrew Kummel**, E Chagarov, M Kavrik,* University of California at San Diego*; M Katz, N Sanford, A Davydov,* National Institute of Standards and Technology (NIST)*; M Lee,* National Taiwan University

The mechanism of stability of the phases of HfO_2, ZrO_2, and HZO ($Hf_xZr_{1-x}O_2$) were systematically investigated with density functional theory molecular dynamics (DFT-MD). For the bulk states, the monoclinic phase ("m") is about 80 mV per formula unit more stable than either the orthorhombic ferroelectric ("f") phase or tetragonal (t-phase) for all three oxides. The surface free energies of the (001), (110), and (111) surfaces of all three oxides were calculated using an identical DFT technique. For all three oxides, the (111) face has the lowest surface free energies consistent with experimental data on columnar HZO grains showing [111] is the preferred growth direction. However, the surface free energy for all direction are nearly degenerate between HfO_2, ZrO_2, and HZO; therefore, even for nanocrystal formation the surface free energy does not favor f-phase formation. The effect of stress/strain was calculated by determining the free energy of formation as a function of the volume of the unit cell. When the oxides are grown in the low density amorphous phase but a post

deposition anneal is perform for crystallization. The crystalline forms are more dense than the amorphous forms and the DFT calculation show that a higher surface area per unit cells will greatly favor f-phase formation. However, the effect is nearly identical for HfO_2, ZrO_2, and HZO; this is consistent with experiments showing the molar volumes of HfO_2 and ZrO_2 being within 2%. Instead, formation of nanocrystalites is hypothesized to be the source of the enhanced processing window for HZO. Experimental data is consistent with partial phase separation in HZO. Atom probe tomography imaging of the chemical composition of TiN/5 nm HZO/Si(001) ferroelectric films show an asymmetric distribution of the Hf and Zr within the HZO layer with the Zr being concentrated near the TiN/HZO interface; this is consistent with ZrO_2 having a 100C lower crystallization temperature than HfO_2 and therefore initiate the crystallization starting on the TiN(111) surface. It is hypothesized that the nanocrystals which template on TiN(111) can produce the interfacial stress/strain needed to stabilize f-phase formation; high resolution TEM shows regions of epitaxial alignment between HZO and TiN consistent with this mechanism. In addition atom probe tomography (APT) was performed on TiN/HZO/Si structures to determine the film composition of the interfaces for indication of possible phase separation of HZO since phase separation could promote nanocrystal formation.

Funding by LAM Research is gratefully acknowledged

10:40am **EM+MP+PS-MoM-8 The Role of Selective Processes in the Atomic Scale Era***, **Robert Clark**, J Smith, K Yu, K Tapily, G Pattanaik, S Consiglio, T Hakamata, C Wajda, A Raley, G Leusink,* TEL Technology Center, America, LLC **INVITED**

The semiconductor industry has reached the point where devices are approaching atomic scales. But continued scaling presents a number of new challenges to our industry. First, there is no longer plenty of room at the bottom, which has forced device makers to scale upward by adopting three dimensional device structures and architectures. This has resulted in a drastic increase in the aspect ratios encountered during chip manufacturing. In addition, even with the advent of EUV lithography it will be necessary to employ multi-patterning technologies in order to fabricate the sub-lithographic features necessary to scale further. Multi-patterning requires multiple masks per layer which presents a challenge in terms of aligning masks to each other within a layer, and from layer to layer as the chip is fabricated. Self-aligned process flows such as self-aligned blocks, fully self-aligned vias, and self-aligned contacts are being employed to increase the margin of allowable edge placement error (EPE) for aligning feature and layers to each other at the cost of additional process complexity as well as exacerbating the problem of ever-increasing aspect ratios. Finally, functional films at useful thicknesses need to be accommodated within the volume of the device without voids or seams that can impact chip yields through degraded electrical performance or by providing a source of particles or foreign material.

To overcome these difficulties it is necessary to begin transitioning from the current top down manufacturing paradigm to a bottom up or additive manufacturing style. Selective depositions and etches represent a path to make this transition for devices makers. Self-aligned process flows already make use of etch selectivity between materials in order to achieve feature self-alignment, but isotropic and anisotropic selective depositions can provide additional advantages. Because area selective depositions are inherently self-aligned to the target material, they can enable new process flows for self-alignment. In addition, anisotropic feature filling can be used to fill high aspect ratio, or reentrant features on the chip without deleterious voids and seems as well as reducing the overburden needed for chemical mechanical polishing (CMP). And selective depositions can also be used to avoid or relieve the crowding of functional films within devices or other structures. In this presentation we seek to illustrate, with examples of new processes currently under investigation, how selective depositions and etches can enable future manufacturing nodes by introducing additive processing into the manufacturing flow.

11:20am **EM+MP+PS-MoM-10 Selective Patterning of Silicon/Germanium Surfaces and Nanostructures via Surface Initiated Polymerization***, **Amar Mohabir**, T Weiss, G Tutuncuoglu, E Vogel, M Filler,* Georgia Institute of Technology

Functional devices (e.g., transistors) require controlled compositional heterogeneity and hierarchy at the nanoscale. When such devices are to be produced at very large throughputs (e.g., large-area integrated circuitry), an alternative to top-down patterning is necessary to define key features. Here, we show how surfaces exhibiting Si and Ge domains can be selectively masked using the surface-initiated growth of polymer films. Our approach is particularly useful for the patterning of, and subsequent deposition on, 3-D nanostructures, such as Si/Ge nanowire heterostructures. Such structures exhibit a variety of exposed facets that complicates direct (i.e., without a mask) area selective deposition approaches. Surface masking of Si, but not Ge, domains is accomplished by attaching an initiator to the surface followed by the atom transfer radical polymerization of polymethylmethacrylate (PMMA). Due to differences in initiator density on the Si and Ge regions, the resulting PMMA is approximately 2x thicker on the Si surface. A subsequent hydrogen peroxide etching step removes PMMA on the Ge surface, thus providing nearly 100% selectivity, but leaves the Si regions unaffected. We hypothesize the mechanism of PMMA removal is hydrogen peroxide diffusion through the polymer layer and etching of the underlying Ge atoms. In this study, we use a suite of spectroscopy and microscopy techniques to investigate the effect of initial Si/Ge surface treatment, PMMA polymerization conditions, and hydrogen peroxide etching conditions on the resulting polymer film properties and surface. The ability to selectively mask nanoscale objects in a bottom-up fashion opens up the possibility for nanoscale patterning in a simultaneously high-throughput and cost-effective manner.

11:40am **EM+MP+PS-MoM-11 Chemically Selective Imaging of Sequential Infiltration Synthesis with nm-scale Spatial Resolution***, D Nowak, **Tom Albrecht**,* Molecular Vista

Area selective deposition (ASD) is an active area of research for advanced nanofabrication. Closely related to ASD is sequential infiltration synthesis (SIS) where inorganic material is infused into select polymer material to render an organic/inorganic hybrid material based on a polymer-template. The organic component can be burned or etched away to leave only the inorganic component, which can be used as etch mask or for other purposes. For lithography applications, the length scale (in nanometers range) and the nature of material (organic and inorganic molecules) are such that traditional techniques such as FTIR, electron microscopy, and X-ray scattering are not able to yield real space, chemically selective imaging of SIS processes. Photo-induced Force Microscopy (PiFM) [1] combines infrared (IR) absorption spectroscopy and atomic force microscopy (AFM) via illumination of the tip-sample junction with tunable IR laser light and mechanical detection of forces acting on the tip in response to absorption of light by the sample. By mapping the IR absorption of the sample as a function of IR wavelength and position, nm-scale resolution is achieved in displaying the locations of heterogeneous materials on the surface of a sample. This imaging capability is useful for investigating chemical pre-patterns as well as selectively deposited materials in area-selective processes like block copolymer directed self-assembly, SIS [2], and a variety of area-selective deposition techniques. In this talk, we will present the PiFM results on a model system: Al_2O_3 SIS using trimethyl aluminum and H_2O with poly(styrene-block-methyl methacrylate) (PS-*b*-PMMA) block copolymer with 41 nm full pitch lamellae, demonstrating sub-10 nm spatial resolution of chemically selective imaging.

[1] D. Nowak et al., Sci. Adv. **2**, e150157 (2016).

[2] Y. Tseng et al., J. Mater. Chem. **21**, 11722(2011).

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