Extending Additive Manufacturing to the Atomic Scale Focus Topic

Room 102B - Session AM+MP+NS-WeA

Atomic Scale Manipulation with SPM

Moderator: Sven Rogge, University of New South Wales, Australia

2:20pm **AM+MP+NS-WeA-1 Advanced Scanning Probe Lithography: Processes, Nanopatterning and Nanoelectronics**, ***Ricardo Garcia***, Inst Ciencia Materiales Madrid, CSIC, Spain **INVITED**

The nanoscale control afforded by scanning probe microscopes has prompted the development of a wide variety of scanning probe-based patterning methods. Some of these methods have demonstrated a high degree of robustness and patterning capabilities that are unmatched by other lithographic techniques. However, the limited throughput of scanning probe lithography has prevented their exploitation in technological applications. Here, we review the fundamentals of scanning probe lithography and its use in materials science and nanotechnology. We introduce several methods, interactions and/or processes such as chemical, mechanical or thermal that enable the tip to modify surfaces. In particular, the presentation is focused on describing the fundamentals and applications of oxidation SPL for nanopatterning and device fabrication of nanoscale field-effect transistors, quantum dots, biosensors and molecular architectures involving a variety of systems from 2D materials to biomolecules; from self-assembled monolayers to silicon.

References

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-Y.K. Ryu, R. Garcia, Advanced oxidation scanning probe lithography. *Nanotechnology* **28**, 142003 (2017).

-A.I. Dago *et al.* Chemical and structural analysis of sub-20 nm graphene patterns generated by scanning probe lithography, *Carbon* **129**, 281 (2018).

3:00pm **AM+MP+NS-WeA-3 Integrated Devices made Using Atomically Precise Advanced Manufacturing**, *D Ward, D Campbell, M Marshall, T Lu, L Tracy, L Maurer, A Baczweski,* ***Shashank Misra***, Sandia National Laboratories

Atomically precise advanced manufacturing (APAM) has enjoyed considerable success in demonstrating high profile physics demonstrations, such as the single atom transistor. However, a considerably broader application space would open up if other transistor elements could be integrated with APAM devices, opening the door to high gain and room temperature operation. However, integration is generally limited by the high temperatures required to prepare pristine silicon substrates for APAM, and by the low temperatures at which phosphorus donors diffuse away once placed into silicon once APAM is complete. Here, we describe progress in integrating metal-dielectric surface gates to achieve high gain, and compensation doping to achieve room temperature operation. The Digital Electronics at the Atomic Limit (DEAL) project is supported by Sandia's Lab Directed Research and Development Program, and was performed in part at the Center for Integrated Nanotechnologies, a U.S. DOE Office of Basic Energy Sciences user facility. Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

4:20pm **AM+MP+NS-WeA-7 Electrical Transport Properties of Si:P δ-layer Devices**, ***Ranjit Kashid***, *X Wang, P Namboodiri, J Hagmann,* National Institute of Standards and Technology (NIST)*; S Schmucker,* University of Maryland College Park*; J Wyrick, C Richter, R Silver,* National Institute of Standards and Technology (NIST)

Si:P has been realized as one of the ideal systems for donor-based quantum computation. Site-selective doping of phosphorous atoms at the atomic scale using Scanning Tunneling Microscopy (STM) lithography on the Si(100) 2×1:H surface enables the fabrication of these devices. In the past, our group has demonstrated that degenerately doped & well confined Si:P monolayers can be fabricated using phosphine dosing and low-temperature Molecular Beam Epitaxy (MBE). In addition, a wide range of 1D and 2D nanoscale devices can be fabricated by combining STM lithography and low-temperature MBE. Here, we present magnetotransport and low-frequency 1/f noise measurements on degenerately doped 1D nanowires, 2D Hall Bars, and van der Pauw structures defined using STM lithography. Specifically, we investigate the dephasing mechanism and present a comparative analysis of transport between STM patterned and mesa etched Si:P δ-layer van der Pauw structures to further elucidate the effects of STM patterning on transport properties.

4:40pm **AM+MP+NS-WeA-8 Atomically Precise Tip Positioning for Automated Writing of Atomic-scale Devices**, ***James Owen***, *E Fuchs, J Randall, J Von Ehr,* Zyvex Labs

Hydrogen depassivation lithography has enabled unprecedented sub-nanometer precision in the positioning of dopant atoms in silicon,[1] advancing the field of silicon quantum electronics. It has also been used for localised atomic layer deposition of Si [2] and TiO_2[3].

In pursuit of our overall vision of Atomically Precise Manufacturing, we are pursuing a number of tactics towards automated fabrication of atomically precise structures. STM lithography vectors are automatically aligned to the surface atomic lattice, and patterns can be input as geometric shapes or arbitrary bitmaps. To improve tip position precision, we have developed real-time creep and hysteresis error correction. Using this, we have previously demonstrated open-loop atomic precision patterning over length scales up to 100 nm. Above this scale, where hysteresis errors are more significant, we are able to reduce the position errors by ~90%.

In parallel with real-time position corrections, we have developed automatic fiducial alignment routines. The tip position can either be aligned to previously-drawn patterns or to deliberate fiducial marks. A large pattern can therefore be stitched together from write fields within which atomic precision can be obtained. Thus, precise patterning can be scaled to large areas.

In the burgeoning field of Quantum Metamaterials[4], large arrays of single dopant atoms are required, with extreme position precision and very high yield. However, the yield of the current thermal process for P limits the yield to 70%[5].

Based on recent work on removal of H from surface PH_2 species[6], we are developing a tip-assisted incorporation process, which prevents the recombination and desorption process. For this application, we need to write single-dimer patterns to adsorb only one PH_3 molecule. For these small patterns, Automated Feedback Controlled Lithography is used, so as to remove exactly the required H atoms from the surface. We are working to improve the detection of the H atom removal, using not only the spike in tunnel current but also the change in the local barrier height [7].

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2. J. H. G. Owen et al., J. Vac. Sci. Technol. B **29**, 06F201 (2011).

3. J. B. Ballard, J. H. G. Owen, et al. *J. Vac. Sci. Technol. B*, **32**, 41804 (2014).

4. J. Salfi, et al. *Nat. Commun.*, **7**, 11342, (2016).

5. J. G. Keizer, S. Koelling, P. M. Koenraad, and M. Y. Simmons *ACS Nano***9** 12537-12541 (2015)

6. Q. Liu, Y. Lei, X. Shao, F. Ming, H. Xu, K. Wang, and X. Xiao, *Nanotechnology*, **27**(13), 135704, (2016).

7. F. Tajaddodianfar, S. O. R. Moheimani, J. Owen, and J. N. Randall, *Rev. Sci. Instrum.*, **89**(1), 13701, (2018)

5:00pm **AM+MP+NS-WeA-9 Kilobyte Scale Data Storage through Autonomous Atom Assembly**, *S Otte,* ***David Coffey***, Delft University of Technology, Netherlands **INVITED**

The ability to manipulate individual atoms by means of scanning tunneling microscopy (STM) opens op opportunities for storage of digital data on the atomic scale. Recent achievements in this direction include data storage based on bits encoded in the charge state, the magnetic state, or the local presence of single atoms or atomic assemblies. However, a key challenge at this stage is the extension of such technologies into large-scale rewritable bit arrays. We demonstrate a digital atomic scale memory of up to 1 kilobyte (8,000 bits) using an array of individual surface vacancies in a chlorine terminated Cu(100) surface. The chlorine vacancies are found to be stable at temperatures up to 77 K. The memory, crafted using scanning tunneling microscopy at low temperature, can be read and re-written automatically by means of atomic scale markers, and offers an areal density of 502 Terabits per square inch, outperforming state-of-the-art hard disk drives by three orders of magnitude.

5:40pm **AM+MP+NS-WeA-11 Extending the Capabilities of STM-based Dopant Device Fabrication**, *T Skeren, N Pascher, S Köster,* ***Andreas Fuhrer,*** IBM Research - Zurich, Switzerland **INVITED**

Since the invention of the first bipolar transistor, integrated circuits have evolved to incredibly complex, ultra-scaled devices with on the order of 10^9 transistors per chip. Even if these devices no longer rely on bipolar technology, excellent control of highly doped regions is still a critical factor for device performance. Moreover, single dopant atoms in a silicon crystal or nanoscale silicon transistors are thought to be candidates for spin qubits with a long spin lifetime.

The hydrogen resist lithography technique is capable of preparing atomic scale planar dopant devices. This is enabled by a large difference in chemical reactivity of the bare and hydrogen passivated Si (001): 2x1 surface. Using a scanning tunneling microscope (STM), the hydrogen layer of the H:Si (001) surface is locally desorbed with nanometer precision, exposing areas of reactive Si. When a gaseous dopant precursor such as phosphine or diborane is introduced, the hydrogen layer acts as a resist and the dopants stick only to the desorbed areas. Compared to conventional fabrication methods, hydrogen resist lithography enables degenerate d-doping with sub-nanometer lateral resolution and abrupt doping profiles.

We have extended the hydrogen-resist technique to p-type doping with diborane and present electrical transport measurements on p-type dopant wires and a simple planar pn-junction fabricated by STM patterning.

In addition, we have developed a CMOS compatible device platform for STM-based atomic-scale device fabrication. The scheme uses pre-fabricated samples with electrical contacts and alignment markers and a hydrogen terminated, reconstructed Si:H(001) surface that is protected from the ambient environment by a capping chip.

The sample surface can be used directly for STM-patterning and atomic device fabrication after in-situ removal of this capping chip. After STM device-fabrication the samples are reintegrated into the CMOS workflow by hydrophobic bonding for wafer scale contacting.

Full functionality of this approach is demonstrated with magnetotransport measurements on degenerately doped STM patterned Si:P nanowires up to room temperature, made possible by the use of silicon on insulator substrates.

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